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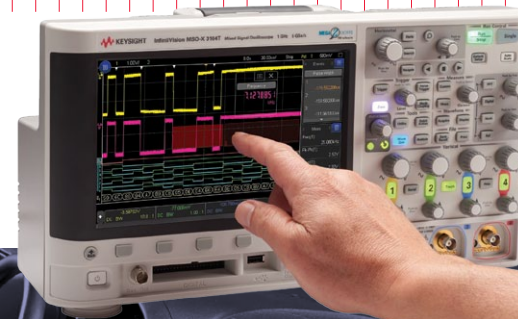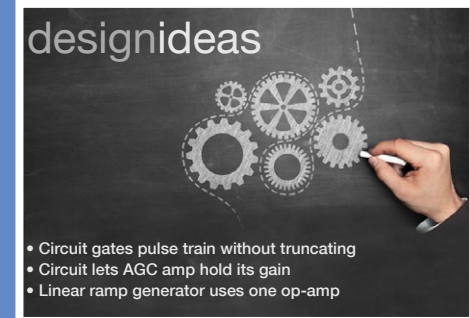*Delivered* RIGHT *Now.*

Keysight's Basic Instruments

February—April 2015

Touchscreen interface makes versatile oscilloscope measurements easier than ever before.

SEE PAGE 3

KEYSIGHT TECHNOLOGIES

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- Circuit gates pulse train without truncating
- Circuit lets AGC amp hold its gain
- Linear ramp generator uses one op-amp

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A plain man's guide to plane waves

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COVER

A little "light" reading; Revise your understanding of plane wave propagation

This month's image is taken from the (full version) of the article that begins on page 30 of this issue. If you have not given any thought to electromagnetic wave propagation since college, this article might provide a novel insight. As the author says;

"If you have studied electromagnetic (EM) field theory, you may know that somehow the electric and magnetic fields in a propagating EM wave generate each other to create a self-sustaining wave. Few people who get that far in their studies can follow the math. Among those who can follow the math, few understand how it works."

FEATUREARTICLES

ONLINE THIS MONTH

EDN's columns

BATTERY, BATTERY, ON THE WALL...

Elon Musk, of Tesla Motors fame, is nothing if not adept at capturing headlines; this time he has done it with his Powerwall concept, of battery-based energy storage for the home. Tesla is proposing to pair local (in-home) energy storage with local renewable-energy capture resources – mainly photovoltaics. Here's the introductory paragraph from Tesla's statement;
"Tesla Powerwall is a rechargeable lithium-ion battery designed to store energy at a residential level for load shifting, backup power and self-consumption of solar power generation. Powerwall consists of Tesla's lithium-ion battery pack, liquid thermal control system and software that receives dispatch commands from a solar inverter. The unit mounts seamlessly on a wall and is integrated with the local grid to harness excess power and give customers the flexibility to draw energy from their own reserve."
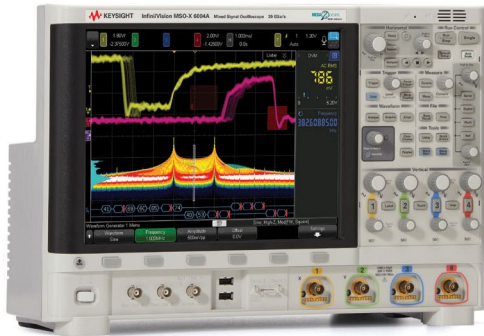The unit will come as a nicely-packaged and styled box to hang on a wall (hence the name) either singly or in multiples. Tesla proposes two basic units, at 7kWh (at around $3000), for load-shifting (store energy when the sun shines, power your stuff by night) and 10kWh ($3500) for continuity through grid outages – in effect, a domestic UPS. These would use the output of the company's "gigafactory", planned, large-scale Li-ion battery production facility.

Tesla has repeated the approach it took with its cars. We know that we simply do not have any electrical energy storage technology that remotely approaches the energy-density of hydrocarbon fuels. Rather than lament the fact that there is no way of replicating the 1000 km-per-tank of a conventional car, Tesla said (in effect) – take what we do have, and maximise its capabilities into a product that people might actually buy. So the Tesla sports car contents itself with modest range, but optimises performance, "kerb appeal" and green appeal.. So with the Powerwall; some quick arithmetic on power densities will show that there's no radically new technology here, but a repackaging of available Li-ion cells into a format that will appeal to consumers already interested in, say, a solar cell installation. EDN Europe readers don't need any help with the maths to show that 7kWh (or even two or three such units) doesn't go all that far. As most of our European readers live on power grids that are less fragile than is the case in some parts of the USA, the attraction of a domestic UPS is probably less relevant. In fact, any examination of battery capacity tables will show that there is not a great deal that could not be done with traditional lead-acid batteries – in kWh/m^3 terms if not in kWh/kg, at least. But as lead-acid is of little use for deep-discharge cyclic operation, the advent of large-scale Li-ion does

have something new to offer in daily-cycling. The hype about capturing energy during the day and running your home from the Powerwall by night may be, more than a little, informed by coming from Southern California/Nevada mindset. If all you have to run to get through the evening is LED lighting, your 60-inch flat screen, a few iPads and a broadband modem, you might be OK; throw any sort of resistive heating or cooking into the equation and the picture becomes rather less favourable. Nor will it "kill the grid", as some of the wilder speculation around the product launch has speculated. In fact, Tesla's proposals depend on charging from the grid, making use of differential (peak/off-peak) tariffs to spread the load for the utility companies, and reduce the cost to the consumer. The Powerwall is unlikely to be a route to large numbers of consumers going "off the grid". It is more about Tesla saying to us, "We've got this large-capacity manufacturing plant due to come on-line that will make rechargeable cells on a new scale and a new price point: and I'll package that in whatever way will each a mass market." (My interpretation, not a quote from Elon Musk himself.) If that leads us, in turn, to conclude that while it's not the battery/energy storage technology of our dreams, we might nevertheless do interesting and useful things with it, that will be no bad outcome.

Welcome to the New Standard.

The next generation of oscilloscope technology.

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Bandwidth	1 GHz – 6 GHz	500 MHz – 8 GHz
Max sample rate	20 GSa/s	20 GSa/s
Industry-leading noise floor*	115 µVrms (1 mV/div)	90 µVrms (1 mV/div)
Plus	– 450,000 wfms/s update rate – Hardware InfiniiScan Zone trigger – 12.1" capacitive multi-touch – 6 instruments in 1 – Voice control	– 10-bit ADC – 100 Mpts std. memory – 15" capacitive multi-touch – Advanced Infiniium GUI

6000 X-Series The new standard in price performance
- Industry's best price performance
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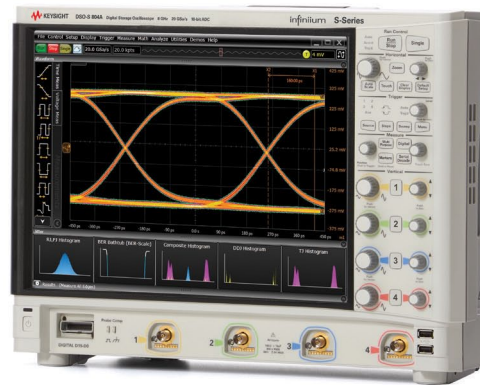
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TECHNOLOGIES

Unlocking Measurement Insights

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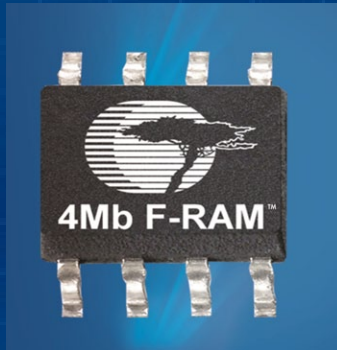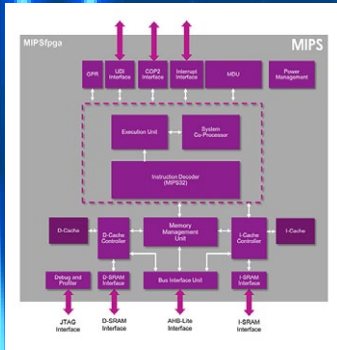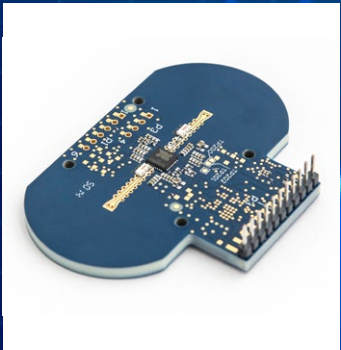
Agilent's Electronic Measurement Group has become **Keysight Technologies**.
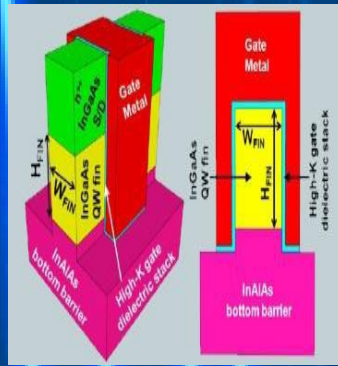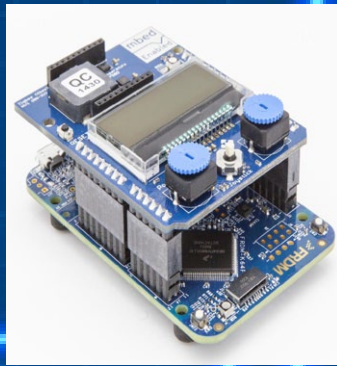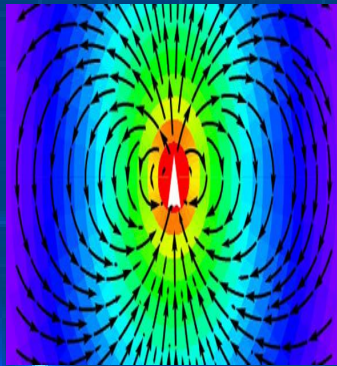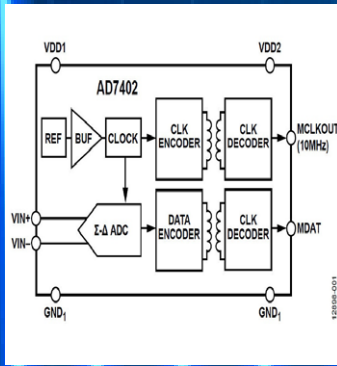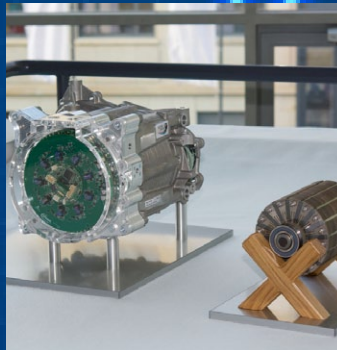
UWB-radar technology senses presence, respiration – in the next room

Norwegian company Novelda has created a sensing technology based on low-power impulse radio techniques which, in its first product releases, it is using to build detection modules for medical, health monitoring and "wellness" applications.

The sensors operate in the international UWB (ultra-wideband) spectrum space, and at the low RF power permitted there, and can implement ranging with millimetre resolution. The company has opted to apply the required signal processing and data interpretation to reduce the "radar return" information to outputs that are specific to (in this case) the respiration-detection application – that is, depth and frequency of breathing.

There are two sensor modules for detecting human presence and monitoring respiration, both based on Novelda's XeThru technology. These can detect presence just from the chest movement while

breathing, and measure both the rate and depth of breathing, allowing breathing patterns to be tracked in real-time. Despite the high frequencies involved, the technology can successfully de-

tect through a variety of objects including lightweight building materials, duvets and blankets to provide non-contact sensing at a range of up to several metres. Lightweight building materials

comprises, for example, internal partition walls. The modules, a company spokesman confirms, can easily detect the movement of baby's chest wall through cot and bedding materials.

The XeThru X2M300 module is intended for smart home automation where its capability for detecting human presence while

being integrated into a building's structure enables hidden, tamper-proof sensing. As well as security and comfort applications, such as the convenient actuation of lighting and environmental controls,

this module can enhance home safety, especially for the elderly or people who live alone, using the absence of normal activity to raise an alarm.

The X2M200 sensor module is designed for respiration monitoring of people of all ages for health and welfare purposes. It is particularly suited for sleep improvement systems and detecting sleep anomalies or other medical conditions. Signal processing and data extraction and interpretation is sufficiently complex that the company has chosen to embed its technology in the application-specific module. In this form, the sensor identifies and provides data on one person – usually, the target closest to the detector. In this sense, it is a one-module-per-person system. Other application domains may follow, for example home (and industrial) robotics. The sensors provide a field-of-view of 60degrees, or 150 degrees at close range (this being the -10 dB angle).

Complete article, here ▶

Imagination lets universities see source RTL for a "real" MIPS core

Imagination Technologies says it is revolutionising education in CPU architectures by introduc-

ing a university programme that gives "free and open" access to a modern MIPS CPU; the MIPS-fpga programme lets universities study MIPS RTL code and explore a real MIPS CPU. As part of the programme participating university departments can get free and open access to a fully-validated,

current generation MIPS CPU in a complete teaching package.

CPU architecture is generally taught as part of electronic engineering, computer science and computer engineering courses, and is based one (or more) of a small number of major CPU architectures. Until now, says Imagination, what's been missing from all of these courses is access to real, un-obfuscated RTL code that will enable staff and students to study and explore a real CPU. Through MIPSfpga, Imagination is providing universities with a simplified version of its MIPS microAptiv CPU core which has been configured by an academic specifically for academic use. Many academics are already familiar with the microAptiv CPU, and it already has a broad ecosystem of support based on its use in numerous commercial products including the PIC32MZ microcontroller (MCU) from Micro-

chip Technology.

The MIPS CPU is being offered as part of a complete free-to-download package for universities, together with a Getting Started Guide, teaching guide for professors, and examples designed to enable students to see how the CPU works and explore its capabilities. With the materials, students can develop a CPU and take it through debug, running on an FPGA platform. This CPU, the company adds, has all the features (MMU, cache controllers, debug interfaces, etc.) required to run a full blown operating system (e.g. Linux). This is contrast to other university programmes where the core is usually encrypted (i.e. a black box) and can only run a simple RTOS.

This MIPS CPU configuration is designed to run on a low-cost FPGA platform, with guides available for the Digilent Nexys4 platform with a Xilinx Artix-7 FPGA, and the Terasic DE2 platform with an Altera Cyclone FPGA.

Complete article, here
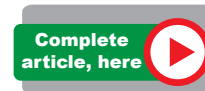
4Mb serial F-RAM for mission-critical data storage

Cypress Semiconductor's ferroelectric RAM range gains a 4 Mbit serial variant that the company positions as expanding the density range of the most energy-efficient nonvolatile RAMs. These serial ferroelectric random access memories (F-RAMs) are, Cypress says, the industry's highest density serial F-RAMs. The 4Mb serial F-RAMs feature a 40-MHz Serial Peripheral Interface (SPI), a 2.0V to 3.6V operating voltage range and are available in industry-standard, RoHS-compliant package options. All Cypress F-RAMs provide 100-trillion read/write cycle endurance with 10-year data retention at 85°C and 151 years at 65°C.

Cypress F-RAMs are suitable for applications requiring continuous and frequent high-speed reading and writing of data with absolute data security. The 4 Mb serial F-RAM family addresses mission-

Inductance-to-digital converters: precise position and motion sensing

Texas Instruments claims a technology first for its multichannel inductance-to-digital converters (LDCs). The four new devices in the LDC1614 family expand the LDC portfolio, a data converter category that TI first introduced in 2013. The devices offer two or four matched channels and up to 28-bit resolution in a single integrated circuit.

The combination of precision and multichannel functionality will allow engineers to design high dynamic range position and motion sensing solutions with simpler system designs and reduced cost, TI says. LDC-enabled inductive sensing employs low-cost, high-reliability inductors as sensors, which can be located remotely from the IC. By integrating up to four channels in a single IC, the LDC1614 family allows designers to distribute sensors throughout a system, while centralising electronics on fewer PCBs. This can benefit precision linear or rotational sensing and metal detection in a variety of end equipments including white goods, printers, cameras and automotive infotainment consoles.

The LDC1614 family offers multiple, well-matched channels, to enable differential and ratiometric measurements, allowing designers to compensate for environmental and ageing conditions such as temperature, humidity and mechanical drift. Precision measurement capability provides up to 28-bit resolution; the devices can detect submicron changes in distance. A wide sensor frequency range supports 1 kHz to 10 MHz operation; designers have flexibility to use many types of inductors as sensors. This frequency range also enables use of very small PCB coils, which reduces overall sensing solution cost and size. Powered by a 3.3-V supply, the LDC1614 family consumes approximately 6.9 mW during standard operation and 0.12 mW while in shutdown mode. For high reliability, contactless sensing is immune to nonconductive contaminants, such as oil, dirt and dust, which can shorten equipment life. The LDC1614EVM evaluation board, which includes the ultra-low power MSP430F5528 microcontroller (MCU), is available to evaluate the LDC1614 for $29. System designers can build sensors with TI's WEBENCH Inductive Sensing Designer. This online tool simplifies sensor coil design based on application and system requirements. The optimised design can be exported to a variety of computer-aided design programs to quickly incorporate the sensor coil into an overall system layout.

World's first multichannel inductance-to-digital converters

- Excellent matching for ratiometric measurements
- Better than 25nm precision
- Reliable and low cost solution

critical applications such as industrial controls and automation, industrial metering, multifunction printers, test and measurement equipment and medical wearables. The company adds that mission-critical systems require high-performance memories that can capture data instantly and reliably on power loss, and that the 4Mb F-RAM family delivers absolute data security.

The 4Mb serial F-RAMs are sampling today in industry-standard 8EIAJ and 8TDFN packages, with production expected in the fourth quarter of 2015.

Complete article, here

Complete article, here

First highly-integrated rare-earth-free synchronous motor

Researchers from one of Europe's largest e-mobility projects have successfully realised a fully-integrated electric vehicle drivetrain without the need for costly rare earths in the permanent
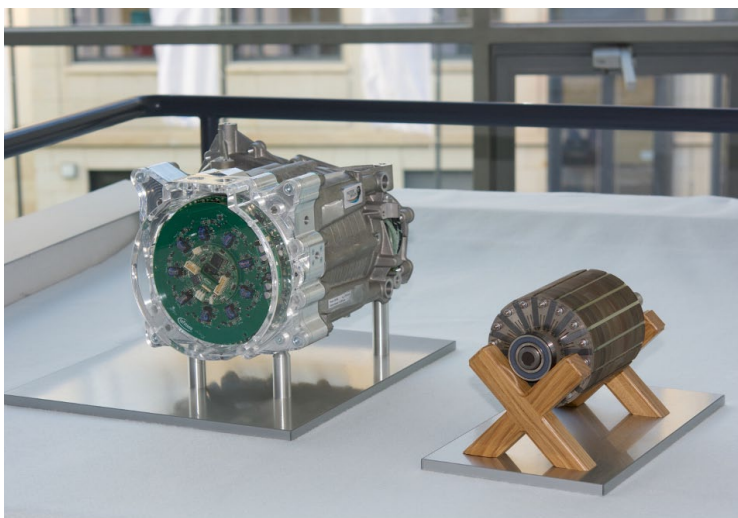
magnet synchronous motor.

Four years ago researchers from nine European countries and more than 30 partner organisations, universities and businesses came together with a single goal: to develop a high-performing and reliable powertrain for electric vehi-

cles that is energy-, resource- and cost-efficient. A large part of the €36million project, dubbed 'Motor-Brain', was dedicated to eliminating the need for rare earth metals in commercially viable engines for hybrid and electric vehicles.

"Rare earth metals produce powerful and reliable permanent magnets, which is why they are used by almost every major hybrid and electric vehicle manufacturer today," says Dr. Yves Burkhardt, R&D engineer at Siemens Corporate Technology and researcher on the EU-funded MotorBrain project. "Yet their availability is limited – around 90% of the world's supply is controlled by China – and they can be difficult and potentially hazardous to mine, making them a key cost driver for electric motors."

The motor sub-team of the project, led by Siemens, immediately discounted induction motors due to limitations in their design and set about investigating alternatives to rare earth permanent magnets in synchronous motors.

"Our results showed that ferrite-based magnets, although inferior to rare earth magnets, could still achieve the same or even better power density than in induction motors but with the other benefits that synchronous motors can offer," Dr. Burkhart says.

For example, the simpler single tooth winding, which can be applied to synchronous motors, requires less wire and the manufacturing process is easier to automate since each tooth can be wound in an identical fashion and pieced

together later. In the manufacture of induction motors, however, the iron ring of the stator must be produced whole with complex windings distributed around multiple lamination teeth. "We can use fewer components and make the manufacturing process quicker and easier. For the end user this means a lighter, cheaper, more efficient motor," he says.

Complete article, here ▶

Multi-function integrated FET switch replaces automotive relays

Infineon's HITFET+ switch family features adjustable slew rate and outstanding protection features; the first family member BTF3050TE is now in high-volume production for replacement of electromechanical relays. The HITFET+ family are protected low-side switches;they comprise highly integrated temperature protected MOSFETs with a feature set including diagnosis function, digital status feedback and short-circuit robustness, and – not available until today – controlled slew rate adjustment for easily balancing switching losses and EMC compliance. The HITFET+ family will comprise at least 16 members varying in RDS(on) (10 to 800 mOhm), feature set (i.e. with and without status feedback), and package size (D-PAK

with 5 or 3 pins, DSO with 8 pins). HITFET+ products of one package size are completely scalable:
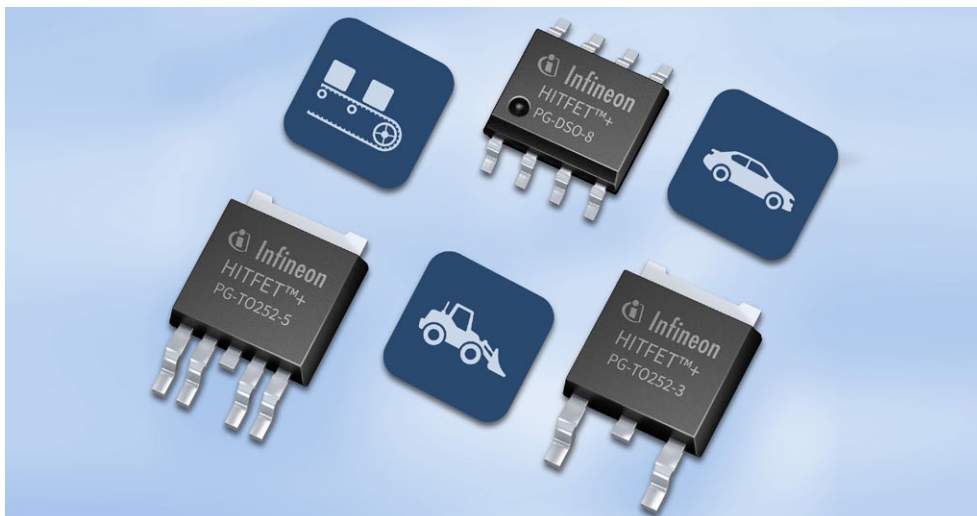
There is no need for system designers to change either software or PCB layout to drive various loads. The first family member, the BTF3050TE, is already available in high-volume.

HITFET+ is aimed at a wide range of automotive and industrial applications whenever there is need for MOSFETs with protection functionality; in automotive applica-

tions, the HITFET+ products can drive solenoids for valve control with PWM (Pulse Width Modulation) up to 20 kHz. They suit automotive light dimming applications where they prevent flickering and support typical power levels of 10W to 60W. The HITFET+ family is suitable for a range of other automotive applications such as mid-size and small-size electric motor drives for door lock or parking brake; for injection valves for alternative fuel (LPG, CNG); flap driving in HVAC (heating ventilation and air-conditioning); rear wheel steering applications as well as safety relay replacement in active suspension systems. HITFET+ products are also suitable as protected drivers in a wide area of industrial applications such as printers; vacuum cleaners; solar power modules; and vending machines.

Complete article, here ▶

Design win; IDT meets IKEA

Integrated Device Technology, Inc. (IDT) has disclosed that IKEA has chosen IDT's wireless power transmitters to embed in its furniture and accessories for convenient wireless charging of enabled portable devices. IDT's P9030 magnetic induction transmitters are embedded in new IKEA products including side tables and lamps.

The products will soon be available in stores throughout North America and Europe. In addition to the furniture, IKEA has developed a line of charging pads as well as a wireless charger that consumers can build into furniture themselves—all built around the IDT wireless power semiconductor devices.

The P9030 transmitter complies with the Wireless Power Consortium's (WPC) Qi standard, delivering a 5W single-chip solution in a compact package. IDT accommodates all major [wireless charging] standards and technologies with

a portfolio of standards-certified products. IDT has proven expertise in both magnetic induction and magnetic resonance technologies, and actively participates in the Wireless Power Consortium (WPC), Power Matters Alliance (PMA), and Alliance for Wireless Power (A4WP) as a board member.

Complete article, here ▶

Distributor RS lists GoPro cameras for 'pro' applications

GoPro cameras are most often associated with "user-generated content"; RS Components is stocking HERO4 Silver and Black cameras it presents as suitable for 'on the job' commercial applications deliver leading-edge high- and ultra-high-definition video at super fast frame rates.

The distributor has two new professional-quality GoPro digital cameras and a wide range of GoPro accessories. The HERO4 Silver and Black are the most advanced GoPro cameras yet, offering high-end performance with built-in connectivity and waterproof durability.

While the cameras are well known for their use in action-packed video in extreme sports and many other consumer-led applications, there is also a place for these products in commercial and industrial environments. For example, site maintenance and installation engineers using cameras to monitor and record daily activities and

inspections.
The HERO4 Silver offers high-definition 1080p60 (1080p at 60 frames per second) and 720p120

video performance with lifelike clarity, as well as 12-megapixel photos at up to 30 frames per second. The camera is also waterproof to 40m (131ft) and offers built-in Wi-Fi and Bluetooth connectivity. The second GoPro camera is the HERO4 Black, which is the most advanced Go-

Pro camera available today. Essentially offering all the features and twice the performance level of the HERO4 Silver model, the HERO4 Black has a more powerful processor and delivers 12-megapixel quality photos at 30 fps and professional-quality video in ultra-

high-definition (UHD) resolution of 4K at 30fps, as well as 2.7K at 60fps and also 1080p120. Like its Silver sister model, the camera is also waterproof to 40m (131ft) and offers built-in Wi-Fi and Bluetooth connectivity.

Complete article, here ▶
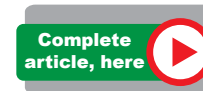
16-bit isolated ΣΔ modulator for HV monitoring applications

Analog Devices has posted details of the AD7402, a high performance, second-order, sigma-delta modulator that converts an analogue input signal into a high speed, single-bit data stream, with on-chip digital isolation based on ADI's own iCoupler (non-optical) technology.
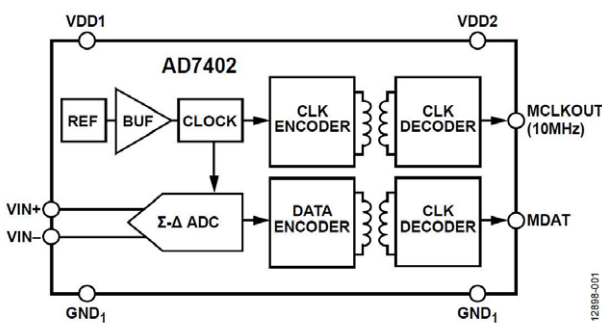
The AD7402 operates from a 5V (VDD1) power supply and accepts a differential input signal of ±250 mV (±320 mV full scale). The differential input is suited to shunt voltage monitoring in high voltage applications where galvanic isolation is required. The input is

continuously sampled by a high performance analogue modulator, and converted to a digital output stream with a data rate of 10 MHz. The original information can be reconstructed with an appropriate digital filter to achieve 87 dB signal to noise ratio (SNR) at 39 ksamples/sec. The serial input/ output can use a 5V or a 3.3V supply (VDD2).

The serial interface is digitally isolated. High speed CMOS technology, combined with monolithic transformer technology, means the on-chip isolation provides outstanding performance characteristics, superior to alternatives such as optocoupler devices.

The AD7402 comes in an 8-lead wide body SOIC package and has an operating temperature range of −40°C to +105°C; it is priced at $3.05 (1000).

Complete article, here ▶

Distribution deal for ARM mbed IoT Starter Kit, with Freescale silicon

A pre-configured ARM mbed-enabled microcontroller development board is now available from distributor element14, hosting an ARM Cortex-M4 processor and IBM's BlueMix cloud service. Farnell element14 has announced it is first to stock the recently launched ARM mbed IoT Starter Kit – Ethernet Edition for IBM Internet of Things Foundation. Priced at £79 (UK Pounds or local equivalent) the development kit aims to enable people with limited or no experience of embedded design or web development to create IoT applications and devices, "in a matter of minutes."

The development kit, which guides users through the processes for

developing cloud-ready IoT devices, comes with an ARM mbed-enabled development board, built on the Freescale FRDM-K64F Kinetis microcontroller, which has an ARM Cortex-M4 processing core running at 120MHz. An Ethernet connection links the kit to IBM's Bluemix cloud service, which acts as a guide on how to use the board. The kits also features a sensor expansion board, which contains a 128 x 32 graphics LCD, 256 kB RAM, 1 MB of flash storage, a speaker, five-way joystick, temperature sensor, accelerometer, potentiometers and a PWM (pulse-width modulation) control line to receive digital signals.

Complete article, here ▶

Antenna-on-a-chip may be feasible, EM research indicates

You may have thought that after more than a century of radio communications, the physics of antenna operation would be entirely understood: apparently not, according to a group of researchers at the University of Cambridge. Their work deals with the mechanisms that launch energy into free space (in transmission) and, reciprocally, capture it from the electromagnetic fields in reception.

One of the consequences of their work is that it appears possible that effective antennae might be fabricated at physical scales comparable to those of integrated circuit dice. That would open up the possibility of a completely chip-scale system, including all elements of RF communication – which would be an enticing prospect for construction of Internet-of-Things "motes".

The work accounts for radiation from conductive antennae, from the widely used but less-well-understood dielectric antennae, and extends it into the use of piezo-electric materials – especially, films – from which the possibility of effective radiation from very small structures emerges.

This note from Cambridge does
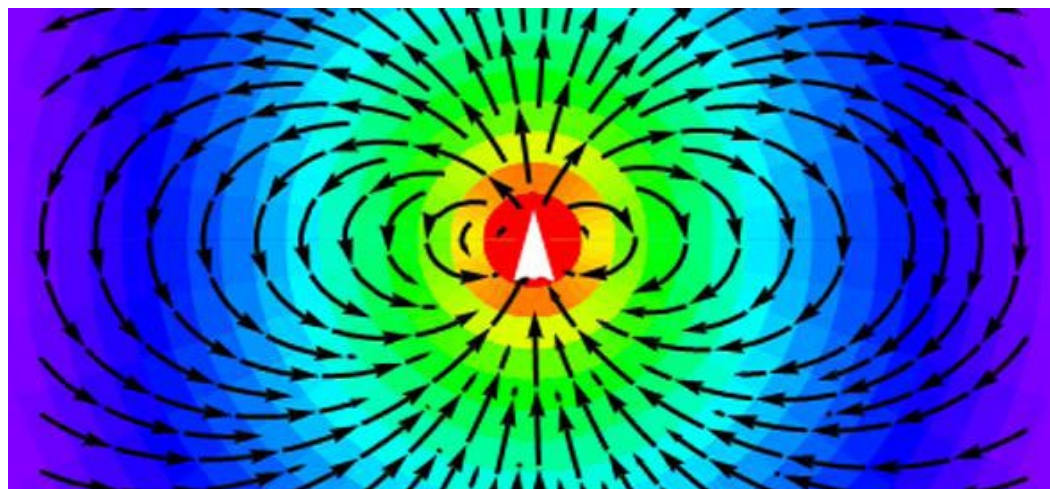
not offer details such as the ratios between physical dimension and wavelength that might be possible, and refers only to "certain frequencies"; it also alludes to resonant behaviour in the piezo materials, possibly implying that any given antenna made this way might be tuned and narrow-band.

The statement issued by the University includes the remarks that, "Another challenge with aerials is that certain physical variables associated with radiation of energy are not well understood. For example, there is still no well-defined mathematical model related to the operation of a practical aerial. Most of what we know about electromagnetic radiation comes from theories first proposed by James Clerk Maxwell in the 19th century, which state that electromagnetic radiation is generated by accelerating electrons. However, this theory becomes problematic when dealing with radio wave emission from a dielectric solid, a material

which normally acts as an insulator, meaning that electrons are not free to move around. Despite this, dielectric resonators are already used as antennas in mobile phones, for example.

"In dielectric aerials, the medium has high permittivity, meaning that the velocity of the radio wave decreases as it enters the medium," said Dr Dhiraj Sinha, the paper's lead author. "What hasn't been known is how the dielectric medium results in emission of electromagnetic waves. This mystery has puzzled scientists and engineers for more than 60 years."

Working with researchers from the National Physical Laboratory and Cambridge-based dielectric antenna company Antenova Ltd, the Cambridge team used thin films of piezoelectric materials, a type of insulator which is deformed or vibrated when voltage is applied. They found that at a certain frequency, these materials become not only efficient resonators, but efficient radiators as well, meaning that they can be used as aerials"

Complete article, here ▶

Bluetooth SIG promotes developer's kit to speed IoT projects

At the Bluetooth World event, the Bluetooth Special Interest Group (SIG) announced beta availability of its Bluetooth Developer Studio, a software-based development kit that cuts developer learning time for Bluetooth technology and dramatically speeds product development. Bluetooth Developer Studio makes building with Bluetooth technology for the IoT – according to the SIG - "simple for developers from the novice to the experienced."

Bluetooth Developer Studio is a graphical, GATT-based application development and debugging tool that could cut Bluetooth education time by up to 50%, with access to tutorials and code samples to jumpstart development. Based on feedback from alpha users and veteran Bluetooth developers, the toolset could shorten development time by as much as 70% (the SIG believes). The Bluetooth Developer Studio's drag and drop functionality lets developers find the Bluetooth profile they need, build on it and create their project quickly. The tool auto-generates code from third-party solutions, such as Bluetooth chip and module suppliers, and can test with both virtual and physical device options.

Complete article, here ▶

Intel's 10nm secrets predicted
By Rick Merritt, EETimes

A semiconductor analyst is making a bold and detailed prediction about the process technology Intel Corp. will use for its next two generations. If he is right, the world's largest chip maker is set to leapfrog the industry once again.

Intel will use quantum well FETs starting with its 10nm process, said David Kanter in an analysis posted on his Real World Technologies Web site. The new transistor structures will use two new materials – indium gallium arsenide (InGaAs) for n-type transistors and strained germanium for p-type devices, he said.

If correct, Intel could gain a capability as early as 2016 to produce 10nm transistors operating as much as 200 mV lower, for lower power consumption, than the rest of the industry. Kanter expects other chip makers will not be able to catch up with the techniques until their 7nm node, at least two years later.

It could take more than a year before Intel discloses its 10nm plans, Kanter said, giving his own predictions an 80-90%confidence level.
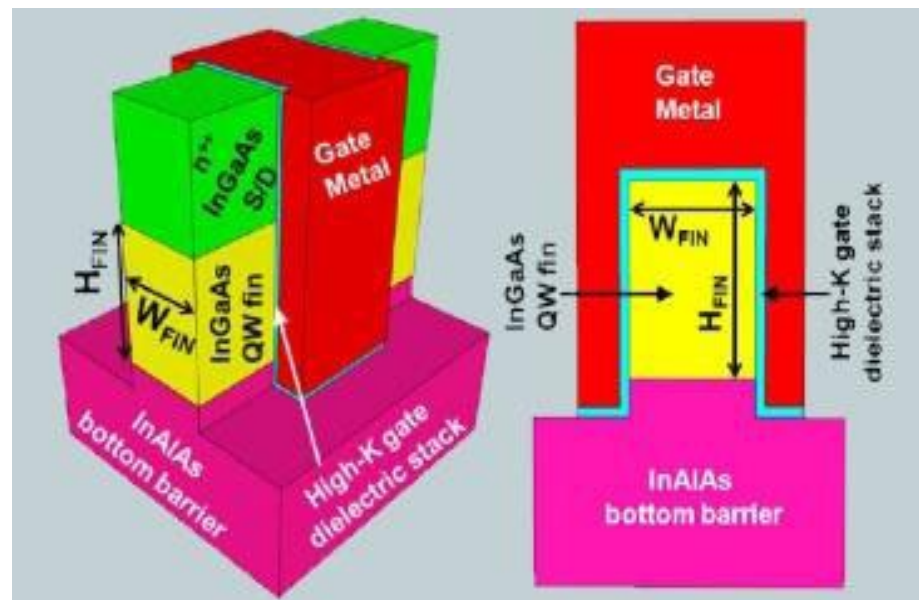
Kanter's analysis is based on a study of about two dozen Intel research papers mainly presented at the annual International Electron Devices Meeting (IEDM), a leading gathering of chip makers. He also analysed as many Intel patents related to chip making.

"Everything I saw pointed in this direction," Kanter told EE Times. "The question is not, 'will Intel do quantum well FETs?', the question is, 'will it be at 10 or 7nm?" he said.

Complete article, here ▶

LeCroy uprates fastest scopes for high-speed electrical and optical tests

Teledyne LeCroy has added enhancements to the two highest performance oscilloscope product lines in the company's portfolio, the 30 GHz WaveMaster 8 Zi in 2009 and the 100 GHz LabMaster 10 Zi.

The LabMaster 10 Zi-A delivers improved performance in effective number of bits and baseline noise along with the industry leading jitter measurement floor. The WaveMaster 8 Zi-B features increased sample rate, lower noise, enhanced processing capabilities and the latest version of Teledyne LeCroy's advanced oscilloscope user interface, MAUI.

The LabMaster 10 Zi-A series includes improvements in signal fidelity and noise performance, underpinning LeCroy's claim of leadership in jitter measurement floor, bandwidth (100 GHz), sample rate (240 GHz) and intrinsic (sample clock) jitter (50 fsec). The WaveMaster 8 Zi-B enhances the capabilities of its predecessor with lower noise, higher sampling rates, deeper acquisition memory, and the next generation of Teledyne LeCroy's MAUI oscilloscope user interface.

Complete article, here ▶

SENSOR FUSION ENHANCES DEVICE PERFORMANCE

By Keith Nicholson, Amithash Kankanallu Jagadish, Bosch Sensortec

With the ongoing revolution in powerful and intelligent device development such as smart phones, new applications are being enabled at a rapid pace and system development often fails to keep up with new and changing requirements. Today, new applications such as indoor navigation and augmented reality, which make use of motion or positional data, require users to accept a somewhat crude sensor fusion implementations originally developed for simple gaming applications. Now, however, end users easily notice the considerable shortcomings and inaccuracies of the implementations.

Sensor fusion is a creative engineering technique that combines sensor data from various system sensors to guarantee more accurate, complete and dependable sensor signals or derived sensory information. For sensor fusion to be consistently accurate it is important to have a deep understanding of the strengths and weaknesses of sensors before the engineer can decide how the data from these sensors is best combined. One approach that is being successfully implemented uses a fusion library based on sensor signals from accelerometers, magnetometers and gyroscopes and compensates for each of the sensor's shortcomings to provide highly accurate, reliable, and stable orientation data.

As end-users become exposed to these new applications, they demand more accurate and reliable solutions. Indoor navigation, where sensors are used to track users between known fixed locations, is similar to early GPS equipment, where only a superior quality of sensor fusion could provide the level of reality, accuracy and therefore user confidence required. OEMs are aware of this and most see this as an opportunity to differentiate their products.

Another example is the progression from virtual to augmented reality. In virtual reality (VR) systems the user is isolated from the real world and immersed in an artificial world. In augmented reality (AR) systems, users continue to be in touch with the real world while interacting with virtual objects around them. With existing technology, the lag in information delivery can actually cause nausea in the user - and such misalignment in AR can result in a very negative user experience.

The big challenge for OEMs and platform developers (i.e. OS developers) is to ensure that all devices deliver the performance required for these applications to work consistently. For example, in Android devices there are many different software and hardware combinations, each resulting in a different output quality. There are currently no standards and no standard test procedures, which means that application developers cannot rely on Android sensor data to achieve consistent performance across many different platforms.

The following is a proposal for a motion tracking camera system to analyse and compare the performance of different hardware/software combinations, and thus set minimum performance criteria. The performance analysis is accomplished by measuring the four key performance indicators (KPIs) of the system:

Static accuracy
Dynamic accuracy
Orientation stabilisation time
Calibration time

The camera-based system produces an orientation vector based on the movement of an object (the smart phone) by tracking markers on the object. Orientation can then be compared with the vectors created by sensors in the phone. These vectors are simultaneously recorded using a data recording application,

which allows a direct comparison of end user devices.

This article introduces the concept of sensor fusion within a smart phone context. It discusses how sensor fusion software is used to improve overall accuracy and introduces a test method including performance result measurement on a number of flagship smart phones.

The fusion library described uses accelerometer, magnetometer and gyroscope sensor signals to compensate for each others' shortcomings and provides highly accurate, reliable and stable orientation data. Let's look at the strengths and weaknesses of these critical devices and how they compensate for each others drawbacks.

The orientation of an object describes how it is placed in the 3-D space and typically the orientation is given relative to a frame of reference specified by a coordinate system. At least three independent values as part of a 3-dimensional vector are needed to describe true orientation. All points of the body change their position during a rotation except for those lying on the rotation axis.

The magnetometer

A magnetometer is highly sensitive to interfering local magnetic fields and distortions, which result in errors in the calculated magnetic head-
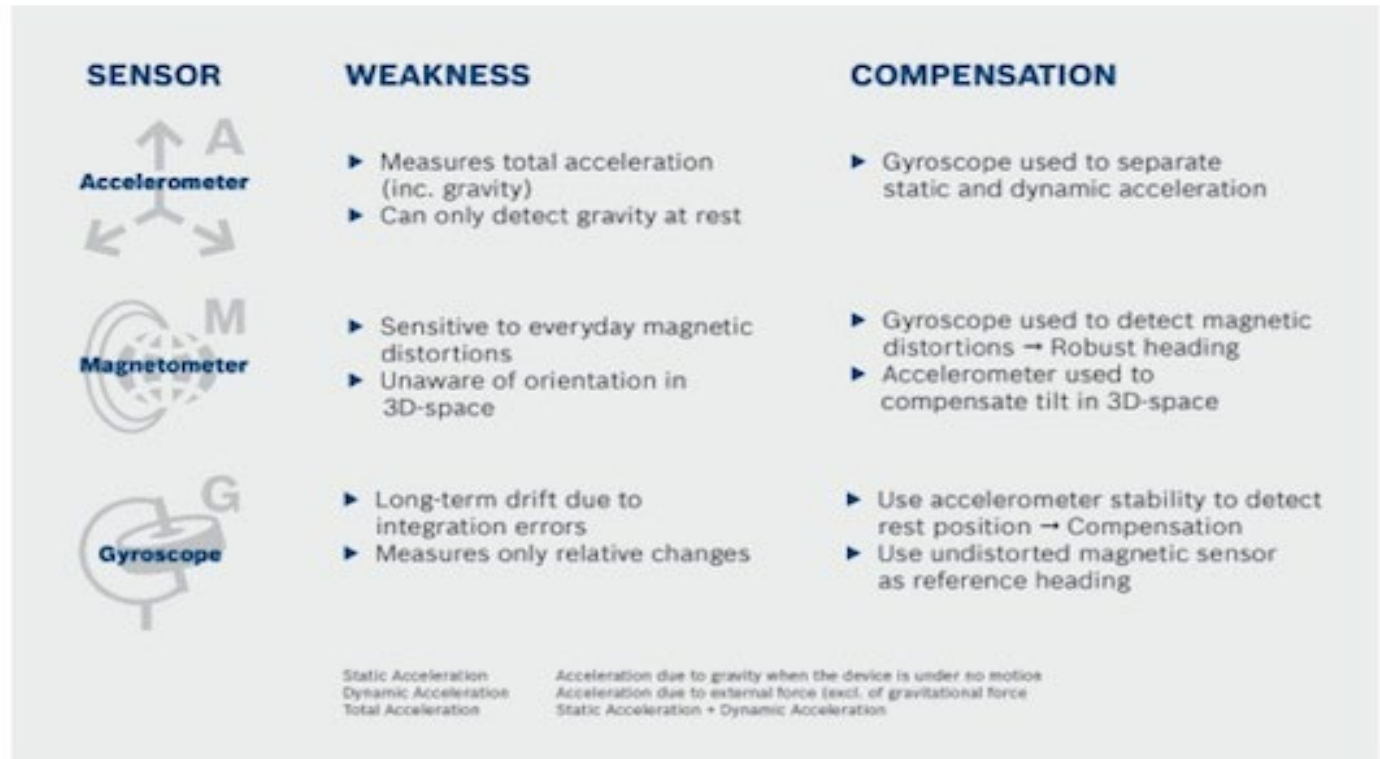
Figure 1. Inherent characteristics of MEMS sensors

ing. The gyroscope can be used to detect such interference and heading changes where no rotation is registered. Sensor fusion can then accurately compensate for this by giving more weight to the gyroscope data than to that of the magnetometer.

The authors continue by outlining the properties of each of the magnetometer, the accelerometer and the gyroscope, and how they are combined in real-world systems; they conclude by showing how error data can be derived to characterise systems performance.

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ADC FULL SCALE RANGE
BY IAN BEAVERS, ANALOG DEVICES

Many analogue-to-digital converters (ADCs) sample a voltage between the true and complement analogue inputs, so they define their input full scale input range (FSR) in terms of a differential (Vpp) or single-ended voltage (Vp), but many system designers really need to know how much input power, in dBm, that the ADC can handle before the input becomes saturated.

The full scale input range of an ADC specifies the largest signal amplitude that can be delivered to the converter inputs before the digital output representation of the signal is clipped. At full scale, the output uses the minimum and maximum codes of the ADC. Some systems seek to maximise dynamic range by using as much of the effective input range as possible, but a saturated ADC will exhibit distortion and poor performance.

Most ADCs have a fixed input impedance; others may provide selectable impedance values. Along with the input voltage, the impedance will determine the input power needed to drive the ADC input to its maximum, so we can convert the full scale voltage from an ADC data sheet to power in dBm, as long as we know the ADC input impedance.

For example, what is the full scale input power in dBm of an ADC with the following full scale input range and input impedance?

ADC full scale input range = 1.0 Vpp = 0.5 Vp = 0.3535 Vrms

ADC input impedance (Rin) = 50Ω

Signal power = $((V_{rms}^2)/R_{in})$ in Watts

$$\text{Signal power} = 10 \log(((V_{rms}^2)/R_{in}) \times 1000 \text{ mW/W}) \text{ in dBm}$$
$$= 10 \log((0.3535)^2/50) + 30 \text{ dBm}$$
$$= 3.978 \text{ dBm}$$
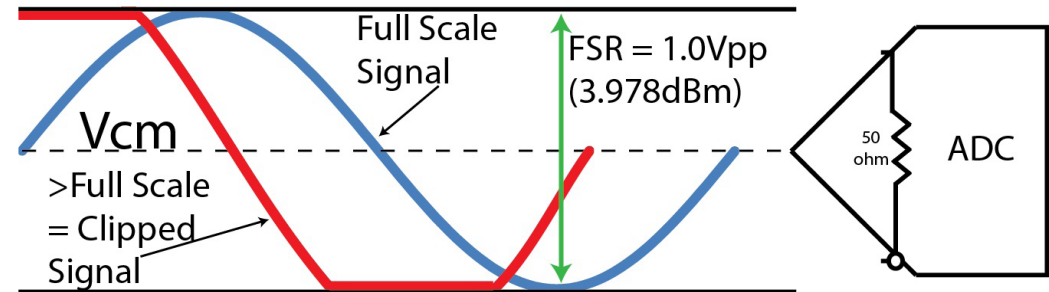
The great things about using input power expressed in dBm are that the values are portable and the math is easy. For example, a doubling of power can be calculated simply by adding 6 dB, and a –1 dB signal with respect to full scale would require an input power of 2.978 dBm for this ADC (3.978 dBm – 1 dB). A frequency domain FFT expresses signal power in dB, so the power at the ADC input can be determined by subtracting an FFT bin power from the full scale power.

An ac-coupled signal to the ADC will be centred about the common mode voltage, Vcm. This will ensure that the maximum signal power can be realised by the ADC without clipping.

A full scale signal will reach the minimum and maximum codes of the ADC, while a signal with increased power will saturate the input and have its digital representation clipped. The power in dBm can be calculated from the full scale voltage and the input impedance.

Ian Beavers [*ian.beavers@analog.com*], *a staff engineer for the Digital Video Processing Group at Analog Devices (Greensboro, NC), is a team leader for HDMI and other video interface products. With over 15 years' experience in the semiconductor industry, he has worked for ADI since 1999. He holds a bachelor's degree in electrical engineering from North Carolina State University and an MBA from the University of North Carolina at Greensboro.*
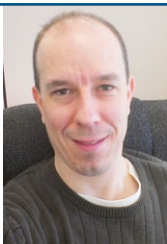
USB 3.1 TESTING PART 2: TYPE-C CABLE ASSEMBLIES

By Randy White, Tektronix

For all of its virtues around plug-and-play device interoperability, USB annoys virtually everyone because if its one-sided cable connector. There's just no easy way to determine which way to plug it in is the correct way, as captured in the cartoon below (Figure 1). The problem is bad enough when you can see what you're doing, say on a laptop or tablet, but things get much worse when you have to crawl under your desktop to plug that new webcam into the back of a tower computer.

Sure, we've lived with the one-sided connectors for two decades so it can't be that bad.
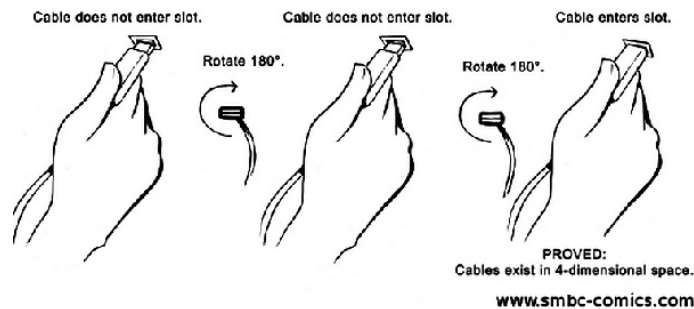
Figure 1. *You have a 50/50 chance of plugging in a USB connector the right way, but get it wrong 75% of the time. Source: smbc-comics.com*

But still, wouldn't it be nice if you didn't have to constantly rotate connectors to plug them in? Enter the new reversible Type-C connector designed to work with USB 3.1 devices. From a design-and-test perspective, there's more to Type-C connectors, but the reverse feature from both sides of the cable (Figure 2) is what has everyone excited.

Much of what's been possible in terms of bandwidth capability for USB results from a well-designed interconnect. In looking at the USB connector's evolution, the standard-A connector that connector to computers is the original flat, rectangular shape. Typically, the standard-B connector at the other end of a standard USB cable plugs into peripheral device such as a printer, phone, or external hard drive. Over the years, a number of variants emerged ranging from the original standard-B to mini-USB and micro-USB as well as USB 3.0 versions.

With the introduction of the Type-C connector, it's safe to say the game has changed. This connector will lead the way to much better user experiences. Indeed, Apple has taken the lead by designing the 12-inch MacBook with one USB Type-C connector that is the only I/O port

Figure 2. *A USB Type-C cable can have Type-C connectors on both ends, making it easy to use.*

on the computer. There was a lot of consideration put into every aspect of typical usage models for mechanical robustness, current sourcing, scalable bandwidth, host or device role swapping, and even supporting other signalling or "alternate mode" as it's referred to in the specification.

Figure 4. *A USB Type-C connector adds duplicate power, ground and data connections that can enhance performance.*

Figure 3. *A USB Type-C connector measures about 8.25 mm side, smaller than a USB 3.0 connector.*

It's worth discussing alt mode. This is a user definable mode that lets you transmit anything you want over the USB cable. One example is DisplayPort, which has now adopted the Type-

C cable as an option. The Type-C connector's flexibility means the DisplayPort alt mode can also choose to transmit on just one or two of the four available signal lanes, allowing remaining lanes for 10 Gbps USB data. Over time, alt mode will be used for a lot of other video, audio, and power applications. It's a bit ironic that on one hand USB is all about standardisation, but with alt mode, implementers can create plug-and-play devices that only work with their brand of devices.

Physically, the Type-C port and connector is most similar to that of the Micro-B USB. Figure 3 compares the USB 3.0 Micro-USB plug to the Type-C plug. A Type-C port measures 8.4 x 2.6 mm, meaning it's small enough for use on even the smallest peripheral devices.

Unlike the Micro-B plug, the Type-C plug has a duplicate set of pins that can be used in either direction. The USB 2.0 differential pair and VCONN pins are duplicated on the receptacle side. As you can see in Figure 4, the Type-C connector has more signals such as RX2 and TX2, plus additional ground pins. These new signals, plus the additional power and ground pins, allow for as much as 100W (20V, 5A) and more intelligent bus configuration capabilities. Looking toward the future, it's not hard to imagine that the duplicate set of pins could be put to use to further boost data transfer throughput through lane aggregation.

The article goes on to discuss the modified definitions of pass/fail testing that will prevail with the updated standard. Click to download the pdf; for part 1 of this article, click here.

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BY BONNIE BAKER, TEXAS INSTRUMENTS

BAKER'S BEST

Complete the simulation of your ADC with IBIS

The easy-to-use successive-approxima-tion analogue-to-digital converters (SAR-ADCs) may not be as easy as you think. In my last article "Simulating the front end of your ADC," (see the March digital edition of EDN Europe, page 19), we talked about macro-models that allow the simulation of the SAR-ADC analogue interfaces (V_{IN} and REF_{IN}).

In the analogue evaluation, the ADC driving amplifier and voltage reference are an integral part of a mixed-signal circuit. In the digital domain, the input/output terminals of the SAR-ADC, connecting digital chips and PCB traces fall into the digital simulation category.

Now, let's go into the digital simulation do-main. It is prudent to be concerned about the integrity of the digital interface, which involves a converter input clock, output data stream, and various digital control signals. If you have not looked at your board-level transmission line overshoot, undershoot, or crosstalk problems, it is possible to inadvertently compromise the signal-integrity of the clock or data signals.

You can anticipate and troubleshoot these types of problems by using digital simulation tools. The PCB's digital signal-integrity relies on timing, voltage-current levels, and parasitics. This is where the digital I/O (input/output) buffer information specification (IBIS) model comes into play.

IBIS simulation
An IBIS simulation provides signal information for an IC device's digital buffers in relation to the PCB traces and the connected digital gate. The IBIS model contains the device buffer's parasitic inductance/resistive/capacitive values, DC current-voltage (I-V) data, and AC voltage-time (V-t) tables. These tables can be exam-ined in the ADS8660 IBIS model, which is also the ADS8881 IBIS model. Texas Instruments collects the data for the IBIS model using the product's SPICE deck, or on the bench. Instead of evaluating precision issues, as can be done with the TINA-TI spice model, use the IBIS model to evaluate digital signal-integrity issues.

The digital interface in Figure 1 could be between the SAR-ADC and the digital host. On the PCB, there are traces or transmission lines that connect these two devices. The basic elements of a transmission line are shown in Figure 1.
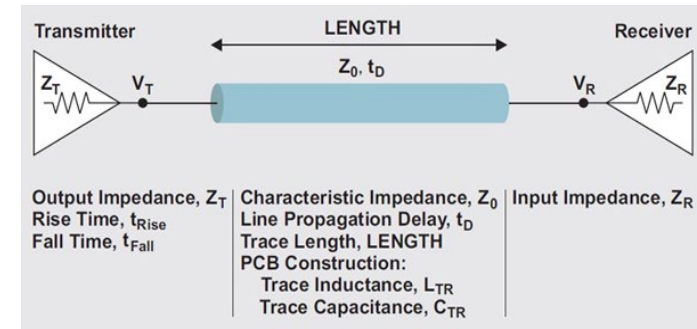
Figure 1 *Here is an example of a single-ended transmission-line circuit. (Ref 1)*

In Figure 1, Z_T is the notation for the transmit-ter's output resistance, and Z_R is the notation for the receiver's input resistance. These speci-fications are not available in standard data-sheets; however, the IBIS model does supply them.

The definition of the transmission line, or PCB trace, includes the characteristic imped-ance (Z_0), propagation delay (D), line propaga-tion delay (t_D), and trace length (LENGTH).

If very little is matching between Z_T, Z_0 and Z_R, the trace is capable of generating electrical ringing. A typical design includes several trans-mission lines on the PCB (Figure 2).

BY BONNIE BAKER, TEXAS INSTRUMENTS

Figure 2 *This is a typical interface configuration between the microcontroller and the SAR-ADC.*

These lines are not independent because of their proximity to each other on the same board. Figure 3 shows an example of ringing in the SCLK and DOUT line, as well as crosstalk between the DOUT and SCLK traces.

Figure 3 *Here there are induced reflections from mismatched termination impedances.*

The IBIS model correctly identifies the problems with this PCB. Additionally, modifying the termination values along with making a PCB trace adjustment on the board corrects these problems (Figure 4).

Figure 4 *Signal integrity problems can be solved with proper termination.*

If the PCB is modeled accurately, IBIS evaluation helps to identify the possible transmission problems that may exist on the board. Once notified of these problems, you can adjust the trace length or location.

Simulation is a tricky thing when it comes to SAR-ADCs. Presently, there is no complete converter model that accurately models the entire device. Resources available are an analogue SPICE file that models the analogue input pin stability, and an IBIS model that assists with finding the PCB signal-integrity problems. For more IBIS information refer to "IBIS Model: A

Conduit into Signal Integrity Analysis, Part 1," and "The IBIS model, Part 2: Determining the total quality of an IBIS model."

Don't get me wrong. Evaluating the details of your ADC prior to designing it in is critical. This is most easily done by studying the product data sheet. Once you do make your final determination, simulation is the next prudent step. The good fortune of having the SAR-ADC TINA-TI spice and IBIS micro-models available is that you now have utensils that address the most critical, difficult converter issues.

References

❶ ADS8860 IBIS model
❷ ADS8860 datasheet
❸ Baker, Bonnie, "The IBIS model: A conduit into signal integrity analysis, part 1," Analog Applications Journal (SLYT390), Texas Instruments, 4Q 2010
❹ Baker, Bonnie, "The IBIS model, Part 2: Determining the total quality of an IBIS model," Analog Applications Journal (SLYT400), Texas Instruments, 1Q 2011
❺ Baker, Bonnie, "The IBIS model, Part 3: Using IBIS models to investigate signal-integrity issues," Analog Applications Journal (SLYT413), Texas Instruments, 2Q 2011

MICROSIP UNWRAPPED; ANATOMY OF A COMPLETE POWER SUPPLY AS SIMPLE AS AN LDO

By Thomas Schaeffner, Texas Instruments

About 10 years ago, a fully integrated step-down converter for an output current of 600 mA was running at a switching frequency of 750 kHz, used a 10 µH inductor and was packaged in leaded plastic packages such as MSOP10. The package itself needed a space of 3 x 5mm, partially because it had leads on two sides. Passive components such as the ceramic capacitors were 1206 size which measure 3 x 1.5mm. The inductor added another 4.5 x 4.5mm and was, with a height of 3 mm, by far the largest component in size and volume. A complete power solution required a board space Inters of 170 mm². Shortly afterwards, QFN packages became standard as they did not need extra space for their pins because they are located under the package and therefore allowed to minimise the space needed for a given pin count. In addition, the PowerPad, an exposed pad on the bottom side of the package, provides a low thermal resistance to the PCB and helps to increase the output power. Along with the progress in passive components, this allowed for the package size to be cut by a factor of 14, down to 28 mm².

A contributor to this progress was the increase in the switching frequency to the 2 MHz range. The inductor became much smaller as the inductance required was reduced to 2.2 µH. As the physical size of an inductor scales with its inductance, a lower inductance means a smaller device. The higher switching frequency also allows the design of power supplies with better electrical characteristics, such as transient response. For a smaller inductance, the

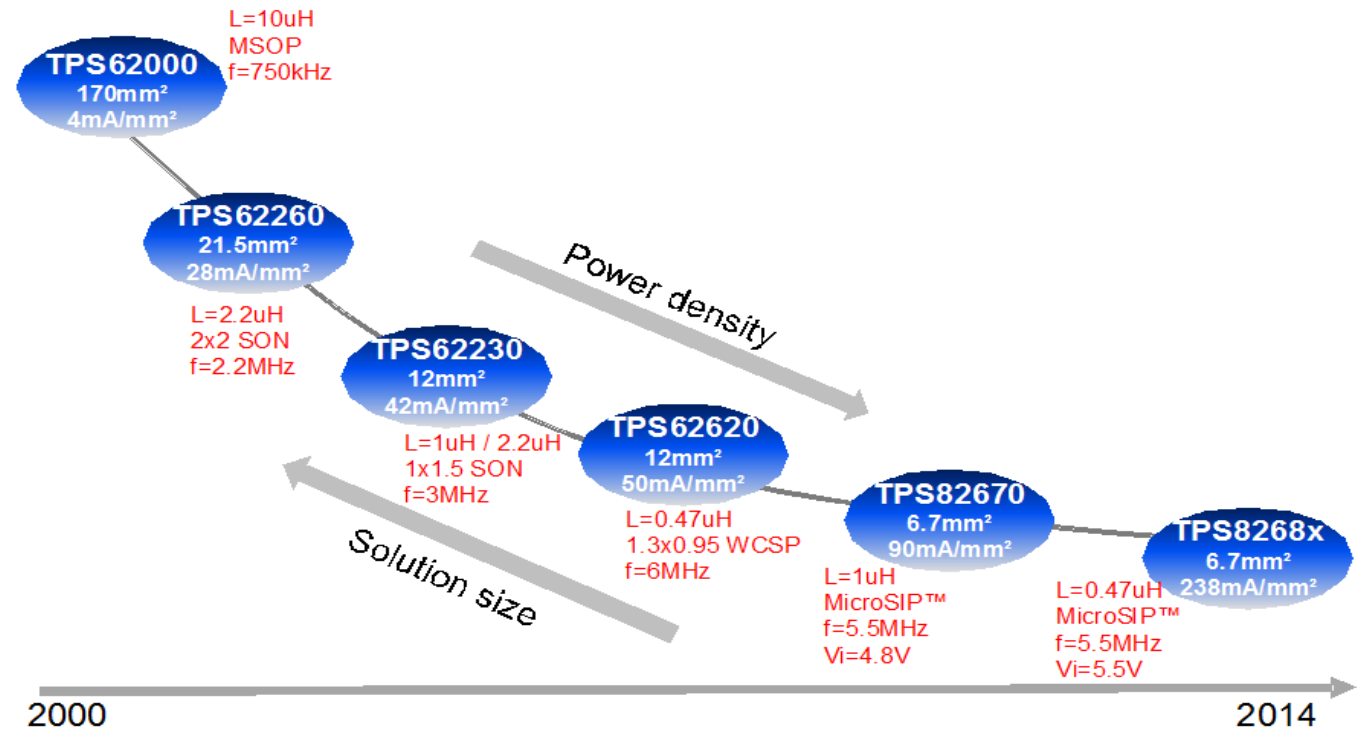**Figure 1.** *Device and package evolution*

current change at a given input/output voltage ratio is larger. This allows a faster reaction to a change in output current. There is a drawback when it comes to losses in the system; switching and magnetising losses scale with the switching frequency.

For these reasons, the majority of converters still operate at a switching frequency in the range of 2 MHz to 6 MHz. The lower frequencies are typically used for applications with a relatively large input voltage, and a focus on high efficiency.

Whereas the higher frequencies have advantages when it comes to the best transient performance; and the smallest total solution size.

The next step in the evolution was to use chip scale packaging for power devices. This reduces the size because there is no package as such. The silicon is just covered on top with a thin tape that contains the marking and protects the silicon from mechanical influences. On the bottom where the active circuitry is located, balls are added which form the electrical connections. Chip scale packaging is the smallest possible. The only disadvantage is that the silicon size needs to be large enough to hold the number of balls required for the electrical connections.
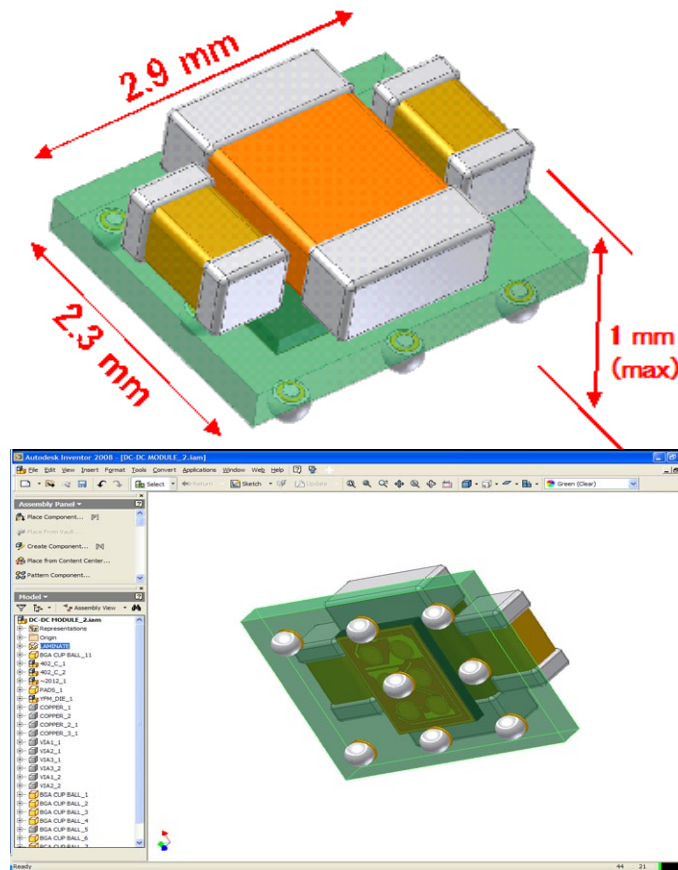

Figure 2. *MicroSIP construction*

For microprocessors it is common practice to stack the memory on top of the processor or even stack multiple dice on top of each other.

Why not do the same thing with the passive components in a switch mode power supply? The TPS82xxx family of devices is going down that route. The passive components are stacked on top of the silicon. However, this is not done directly on the silicon but the silicon is embedded into a PCB, which in turn holds the passive components.

Applications that require small solutions typically also care about the volume, not only the area. As such, a solution has to be competitive with discrete solutions with respect to height.

The MicroSIP modules in the TPS82xxx family provide a total solution size of 6.7 mm² at a height of 1 mm maximum. This is achieved by packaging the silicon inside a 300 µm (0.3 mm) thick PCB which has the passive components on top and balls similar to WCSP or BGA packages on the bottom. This means the module can be picked, placed and soldered like a BGA package.

This allowed shrinking the solution size to roughly half that of a discrete solution; *the article continues with an illustration of the difference between the discrete solution and the MicroSIP version*

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NEW DEMANDS ON DC-LINK POWER CAPACITORS

By J.Konrad, M. Koini, M. Schossmann, M. Puff, EPCOS OHG

Following the trends in power electronics both automotive and industry applications need compact, reliable and cost effective components to reach the major targets of increased power density and miniaturisation. Key technologies such as fast switching semiconductors are already successful .

Since electronic components and their characteristics become more and more complex, design solutions have to be found on the system level and in addition, the interaction of active and passive devices needs to be understood in detail. The DC-link capacitor – as part of the commutation loop and especially during semiconductor switching – has a lasting effect on the behaviour and efficiency of the application. Different power electronic designs use low inductive assemblies of semiconductors and DC-link capacitors to lower the voltage overshoot during turn-off [4]. In most cases, system designers have to deal with capacitors of large volume and with large commutation loops. The "CeraLink" capacitor technology which is described in this paper and was introduced earlier in [1] and [2], shows high capacitance density as well as a very low self-inductance to keep the commutation loop inductancelow.

DC-link capacitors in power electronics

DC-link capacitors are used in most power converters to stabilise the DC-link voltage by balancing the interim difference between the input source and the output load. The voltage ripple needs to be minimised to avoid electrical stress to the source and semiconductors as well as to comply with EMI requirements. It also acts as energy storage during the hold-up time. Besides its major function, a DC-link capacitor should contribute to fast and efficient switching of the semiconductor by minimising the necessary space.

To a large extent, the packaging and outline of a motor inverter is defined by the DC-link capacitor size [3]. Therefore high capacitance density is a major key parameter in any effort to decrease the inverter volume and to increase the power density. Together with a high current handling capability, a low self-inductance and an optimised connection technique, a compact DC-link is a desirable attribute. This principle is also true for other power electronic converters,
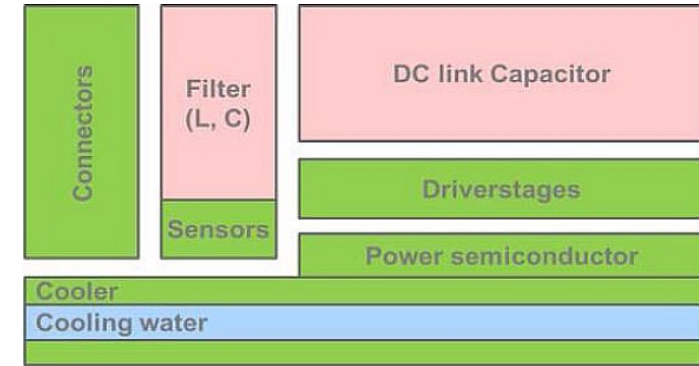
Figure 1. *principle block picture and size comparison of a motor inverter (source: Volkswagen AG [3])*

where a miniaturisation of the DC-link capacitor is needed. Additionally, robustness requirements must be fulfilled for defined stresses (thermal, electric, environmental, and mechanical). Therefore, new developments in DC-link capacitor technologies have to focus on the demands of next generations of power electronics.

Device characteristics: Ceramic material

The continuation of this paper describes a new capacitor technology, "CeraLink", that contains lead-lanthanum-zirconate-titanate ceramic (PLZT) as dielectric material ([1], [2]).

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Spin Cycle

Simplify complex control problems using disturbance rejection

By Adam Reynolds, LineStream Technologies

Control systems using the traditional PID approach need either robust system modelling or extensive empirical tuning to achieve optimum results. An alternative approach has become available, however, that can simplify control system tuning to as little as one parameter. Called active disturbance rejection control (ADRC), this approach can compensate for changing system parameters in real time.
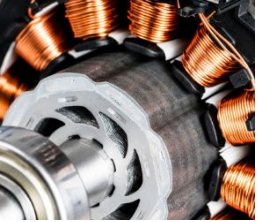
Consider, for example, an industrial winding machine. Winders are used in manufacturing paper, plastic films, metals, wire and textiles. These products are then used in other manufacturing processes, such as packaging and printing. Winders must produce tightly wound, uniform rolls of material to ensure the follow-on process' success.

Figure 1 depicts a winder. A speed controller is used to drive the motor spindle on which the material is wound. Position controllers are used to hold the dancer arms in the vertical position shown in the diagram. The dancer arms control the tension of the material as it is wound on the spindle.

Winders are notoriously difficult to control due to constantly changing dynamics. The first challenge is that the material being wound may have deviations in quality. The position controllers for the dancer arms must control the tension equally well across varying product quality so as not to distort the product. For example, when producing thin plastic film, there are
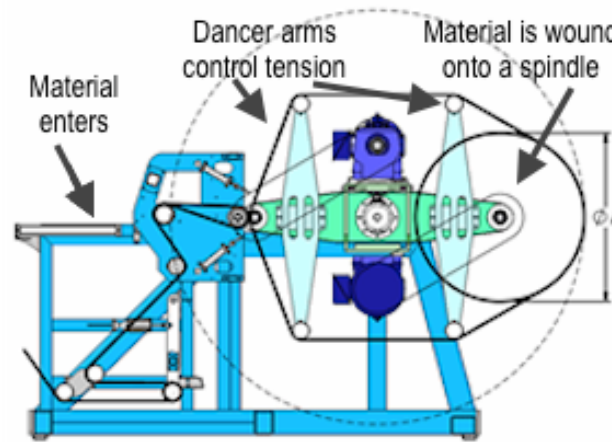

Figure 1 *Essential elements of a winder system.*

variations in resin quality, and these imperfections must not be amplified during the winding process.

The second challenge is that the inertia of the winder's motor shaft changes by an order of magnitude as the spool transitions from empty to full. The tension must remain constant as the material is wound. It is fairly easy to maintain the correct dancer position when the motor spindle is empty, but control of the dancer arms becomes more difficult as the spool of material grows. It is also difficult to control the dancer arm position as the winder accelerates and decelerates.

These dynamic changes during the winding process are very difficult to tune and control with standard PID-based control. PID-based methods can only be statically tuned for single snapshots of an evolving system. Adequate PID tuning for winder applications requires significant time and expertise.

Active Disturbance Rejection Control (ADRC), however, can actively compensate for changing conditions, such as inertia changes and material imperfections. Traditional PID control simply reacts to deviations in a system's output from a desired setpoint by applying a correction signal based on a system model or tuned to a specific system configuration. That correction is a linear combination of the error term, its rate of change, and its time integral (to correct for a DC bias). ADRC works by actively estimating what is disturbing the system from its desired behaviour, including changes within the system itself. It compensates for that disturbance using a non-linear combination of error terms. (For a detailed description of ADRC, see From PID to Active Disturbance Rejection Control by Jingqing Han.)

This column continues with a comparison of the ADRC control technique with PID, using LineStream Technologies SpinTAC Motion Control Suite.

Complete article, here ▶

TEAR DOWN: THE PROPAGATING PLANE WAVE

By Roy McCammon, 3M EMD L&M Laboratory

Using the underappreciated fields

If you have studied electromagnetic (EM) field theory, you may know that somehow the electric and magnetic fields in a propagating EM wave generate each other to create a self-sustaining wave. This can be proven using vector algebra, partial derivatives and curl. Few people who get that far in their studies can follow the math. Among those who can follow the math, few understand how it works.

This article will show with pictures how the fields of a plane wave interact to generate each other with almost no math. To do this, we will introduce two ideas that may be unfamiliar to some readers. The first idea is that $\partial\mathbf{D}/\partial t$ and $\partial\mathbf{B}/\partial t$ (the underappreciated fields) are legitimate fields and should be treated as such. In particular, it is useful to depict these fields along with $\mathbf{E}$, $\mathbf{H}$, $\mathbf{B}$ and $\mathbf{D}$.

The second idea is that a current composed of magnetic monopoles would be associated with the $\mathbf{E}$ field in the same way that a current of electrons is associated with the $\mathbf{H}$ field.

You already know that sending current through a wire coiled into a solenoid shape can create a strong magnetic field inside the solenoid. We will build on that knowledge. But before we do that, we need to define some symbols.

Definitions:

$\mathbf{E}$	Electric Intensity
$\mathbf{D}$	Electric Flux Density or Electric Displacement Density
$\mathbf{H}$	Magnetic Intensity
$\mathbf{B}$	Magnetic Flux Density or Magnetic Displacement Density
$\partial\mathbf{D}/\partial t$	Electric Displacement Current Density
$\partial\mathbf{B}/\partial t$	Magnetic Displacement Current Density

The word *cause* (and related words such as create or generate) will be used in a loose manner. For instance, if we were talking about ohms law, $V = I \cdot R$, it might be convenient to say that the current causes the voltage or it might be convenient to say that the voltage causes the current. Given R, current can be derived from voltage or voltage can be derived from current. We will say X causes Y or X creates Y because that is the language we normally use, but we will mean that X and Y have a relationship such that complete knowledge of X mathematically implies complete knowledge of Y and that the result would be the same if X were the actual cause of Y.

> *"Few people who get that far in their studies can follow the math. Among those those who can the math, few understand how it works."*

We also need to lightly cover a few unfamiliar topics.

• **Magnetic Current**: Ostensibly, a current composed of moving magnetic monopoles. Just as electric monopoles (electrons for example) in motion constitute an electric current, magnetic monopoles (if they existed) in motion would constitute a magnetic current. There are no magnetic monopoles; but if there were, Maxwell's equations are readily extensible to include magnetic charge and magnetic currents. Sometimes, when analysing antennas or other EM field problems, the problem can be made easier by transforming the problem to its dual. This can give rise to non-physical magnetic currents. Harrington[1] discusses the generalized Maxwell's equations and Balanis[2] discusses how magnetic currents are sometimes used to analyze antennas. Just as electric currents are accompanied by a magnetic ($\mathbf{H}$) field, mag-

ELECTROMAGNETICS

netic currents are accompanied by an electric (**E**) field. Magnetic current following a solenoid path would create a strong **E** field inside the solenoid analogously to an electric current following a solenoid path creating a strong **H** field inside the solenoid. *All you need to know about magnetic currents is that they are just like ordinary electric currents except they are accompanied by an **E** field instead of an **H** field.*

• Displacement Current Densities: You may know that $\partial\mathbf{D}/\partial t$ is called the electric displacement current density. You may have never heard of a name for $\partial\mathbf{B}/\partial t$ but you probably would not be surprised to know that it is called the magnetic displacement current density. The value of $\partial\mathbf{D}/\partial t$ field at a particular point in space and time is the partial derivative of **D** with respect to time at that same point in space and time. $\partial\mathbf{B}/\partial t$ has a similar relation to **B**. According to textbooks and from where they occur in Maxwell's equations, we know that $\partial\mathbf{D}/\partial t$ and $\partial\mathbf{B}/\partial t$ act exactly like an electric and magnetic current densities respectively. A classical vacuum is empty, so it may seem paradoxical that there could be a current in the vacuum. It may seem doubly paradoxical in the case of magnetic displacement current. Not only is there a current in a supposedly empty vacuum, but it acts like it is made of non-existent magnetic monopoles. In classical physics, there is no satisfactory physical explanation as to the

composition of these fields in a vacuum. We will take the pragmatic approach and simply say that if the **D** and **B** fields exist, then the $\partial\mathbf{D}/\partial t$ and $\partial\mathbf{B}/\partial t$ fields also exist and can be illustrated in the same manner as any other field. *All you need to know about $\partial\mathbf{D}/\partial t$ and $\partial\mathbf{B}/\partial t$ is to consider them to be ordinary electric and magnetic current densities respectively.*
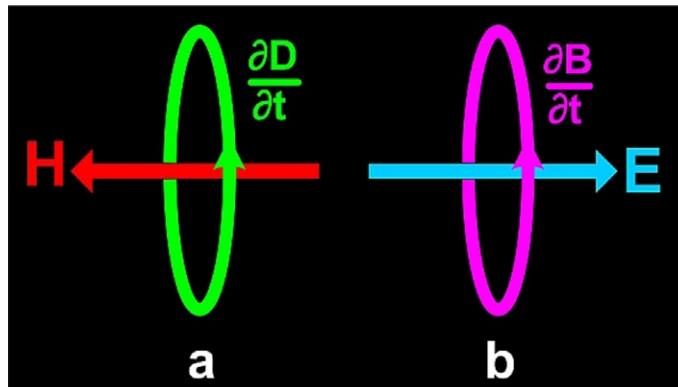

Figure 1. *Displacement currents as sources of E and H.*

Fig. 1 depicts the displacement currents and the fields that they create. There is an asymmetry in the handedness of the fields. In fig. 1(a) when $\partial\mathbf{D}/\partial t$ creates **H**, it follows the right hand rule. In fig. 1(b) when $\partial\mathbf{B}/\partial t$ creates **E**, it follows the left hand rule. This asymmetry is

essential. Without it, the plane wave would be self-extinguishing instead of self-sustaining.
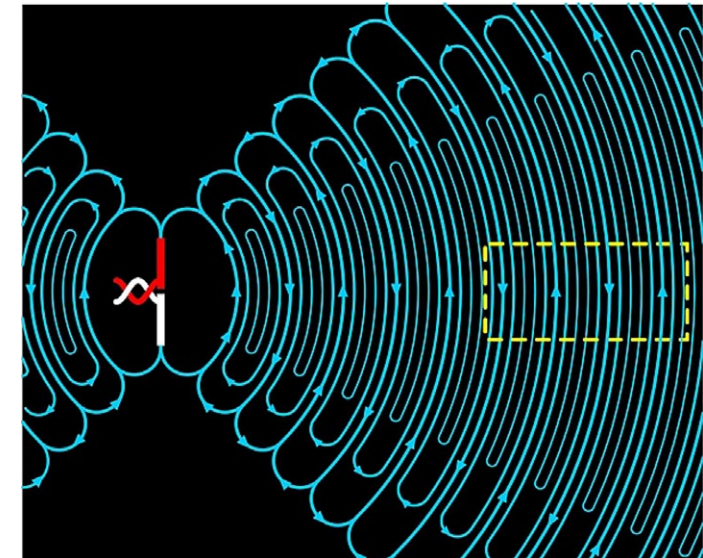
Figure 2. *Side view of the E fields radiated by a dipole antenna*

The article continues by applying this perspective to fields radiated by a dipole antenna (Figure 2, above) to aid comprehension of how the propagating plane wave is generated – click below.
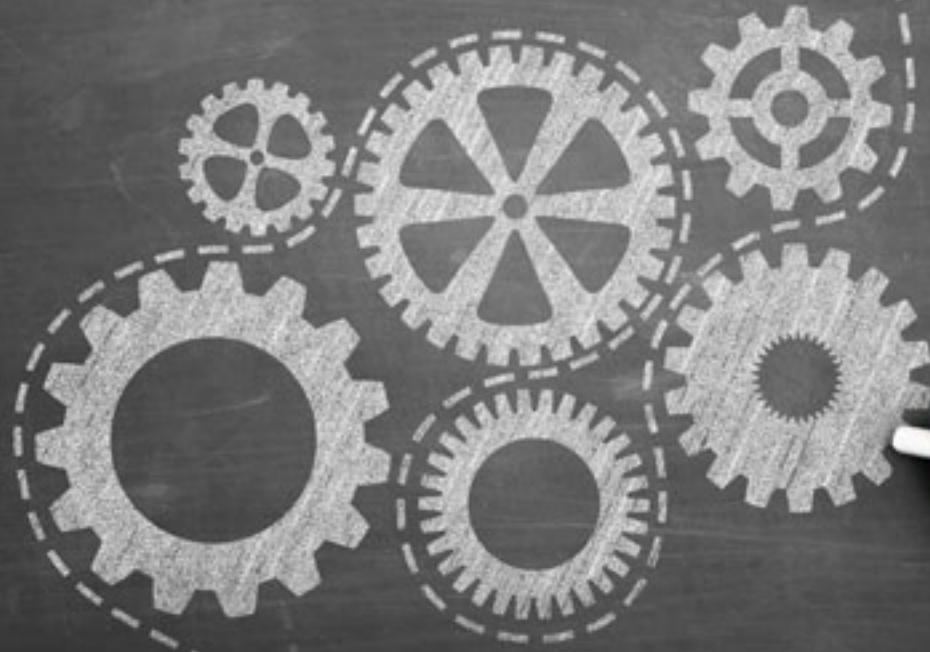
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designideas

- De-embed transmission lines with FIR filters
- Rotational (or linear) measurement using an optical mouse sensor

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De-embed transmission lines with FIR filters   By Mohit Kumar

    Serial data rates out of networking SERDES have reached as high as 28 Gbps and are continuously evolving. At such high data rates, even small PCB traces act as transmission lines, degrading the signal integrity through attenuation and dispersion. It is difficult to monitor the SERDES transmitter output right at the chip balls. Usually, the signal will be brought to an SMA or SMP connector to be monitored by oscilloscope. However, the signal characteristics change due to the transmission line present between the IC and the connector. The challenge is to monitor the signal performance at SERDES pins, and this can be accomplished by de-embedding the effect of the trace. This Design Idea describes a methodology to de-embed the transmission line.

Let H(s) be the impulse response of the trace, if X(s) is the input signal, mathematically:

$$Y(s) = H(s) * X(s)$$

$$X(s) = Y(s) * H^{-1}(s)$$

We can implement $H^{-1}(s)$ as an FIR filter, using MATLAB to determine the filter coefficients (link to files at end of article).

The H(s) of a trace can be measured using a network analyser by measuring Sdd21. We need to determine the coefficients of an FIR filter ($h_f(t)$) whose frequency response($H_f(s)$) is close to the inverse of Sdd21 measured above, i.e., $H_f(s) = H^{-1}(s)$. The approach used to compute the filter coefficients is to start with certain coefficients and compute the frequency response. Compute the error magnitude between H(s) and Hf(s). Using an optimisation algorithm, coefficients are varied to minimise the sum-squared error.

Referring to *FIR_filter_design.m*, **nc** is the number of coefficients in the FIR filter, and **drate** is the data rate in Gbps of the input serial data. Choose **fs** such that **fs/drate** is an integer. This will define the number of coefficients present in one bit. **ncbit** gives the time difference between the adjacent coefficients. Let **N** be the number of points in the frequency response $H_f(s)$, and **numfpts** = N/2 is the number of frequency points in the Nyquist range. The Nyquist frequency for the filter transfer function is **fs**/2. Define a frequency range **finmin** to **finmax** over which the magnitude error is computed.

Frequency points up to the Nyquist for the filter are given by:

$$Hz_1 = (k*\mathbf{fs})/(2*\mathbf{numfpts}), \text{ where } k = 0 \text{ to numpts-1}$$

Interpolation is done to compute the Sdd21 magnitude at Hz_1 frequency points. Initialise filter coefficients to some value. Compute the magnitude of the frequency response of the filter using **freqz** MATLAB function, and determine the error between the Sdd21 magnitude data obtained after interpolation. The sum square error is minimised using the MATLAB **fminbnd** function. The minimisation algorithm can be implemented in many ways; the code presented here is only one way of implementing it.

Experimental results
To demonstrate the effect of the FIR filter, a Keysight 86100D sampling scope is used, along with a Tektronix BERTScope, generating a pattern at 10.3125 Gbps. The output of BERTScope is connected to the DSO, and the waveform is stored in the scope memory, as shown in Figure 2 (magenta). The BERTScope output is then connected to a transmission line on a PCB; the SDD21(dB) profile of the channel

is shown in Figure 1. The output from the channel is connected to the DSO (yellow trace). The attenuation and dispersion caused by the channel have significantly degraded the waveform. In the math option of the scope, there is a linear equaliser block which takes filter coefficients as input. Insert the linear equaliser block in the signal path and enter the filter coefficients. The output of the block is the green trace. The FIR filter removes the ISI effect of the channel and restores the waveform quite well.
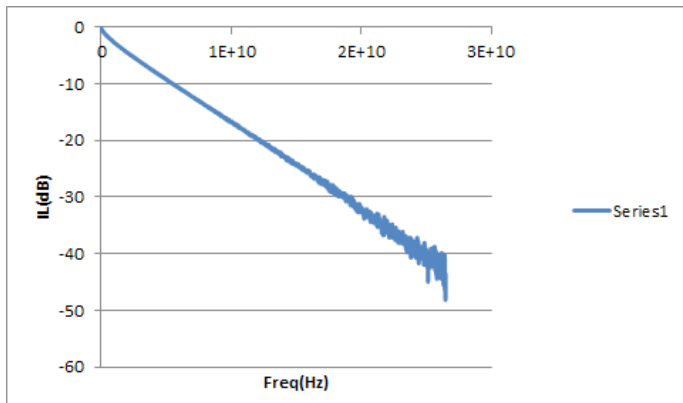

Figure 1. *Sdd21 of the PCB trace*

The FIR coefficients obtained from the MATLAB code are:

0.766, -0.115, -0.097, -0.119, -0.090, -0.099, -0.083, -0.033, 0.028, 0.015, 0.042, 0.013, 0.024, -0.008, 0.002, -0.019, 0.000, -0.025, 0.005, -0.014, 0.011, -0.007, 0.021, -0.002, 0.014, -0.009, 0.009, -0.018, 0.003, -0.022

Figure 2. *BertScope PRBS7 output (magenta); signal at PCB trace output (yellow); FIR filter output (green)*

The filter has significantly improved the signal integrity by removing the attenuation caused by the PCB trace. Processing can be done in an oscilloscope, offline, implemented in hardware, etc.

There are some differences between the BertScope output and filter output, which could be due to the following:

There is some peaking in the first UI. This is due to the large values of filter coefficients a2, a3, and a4. Most of the high frequency amplification is done by these coefficients, which causes the peaking. The algorithm could be modified to correct this.

H1(s) should be band-limited by using a LPF function. This will give a band limited filter and the error should be minimised over the entire transfer function. This is also expected to reduce the peaking in first UI. In this article, the filter is band-limited by defining fmin and fmax, which introduces errors.

The phase information is not included in determining the filter coefficients, which introduces some errors.

Calculation of the filter coefficients could be improved by making these corrections in the design algorithm.

Download the Matlab files (zipped archive) from here.

designideas

Rotational (or linear) measurement using an optical mouse sensor

By Anatoly Besplemennov

This Design Idea utilises an optical computer mouse's sensor for measuring rotation of a disc which can be mechanically connected to any sort of rotating apparatus. One feature is to allow adjustment of the pulses per revolution by changing the sensor's position along the disk radius.
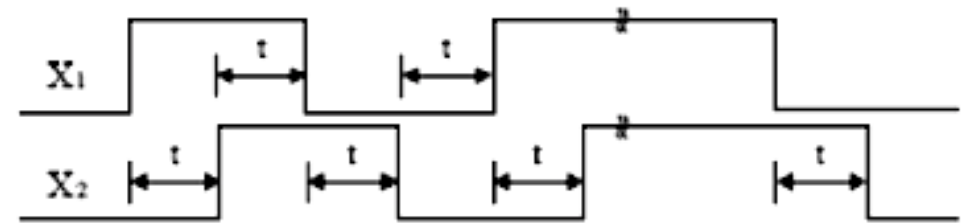
The CMOS optical sensor of the mouse chip provides a non-mechanical tracking engine. Inside the chip, images are captured, digitised, and digitally processed.

For instance, let's consider the simple and low cost OM02. The sensor measures position by acquiring surface image frames and mathematically determining the movement direction and value. The sensor is mounted in a polystyrene optical package and is designed to be used with a high intensity LED. It provides a complete and compact tracking engine. It has no moving parts and requires no precise optical alignment. The OM02 produces a quadrature output for both X and Y directions of movement. The resolution is about 0.0025 inches (0.064mm), and the motion speed, up to 16 inches per second (40 cm/sec).

The IC generates a quadrature X-direction output signal which emulates an ordinary encoder's output. Both X & Y can be used for a 2D system. X1 and X2 quadrature signals are generated at a maximum frequency of about 25 kHz. The following diagrams show the timing for positive X motion (to the right direction). The quadrature output can be used for direct stepper motor control if needed.
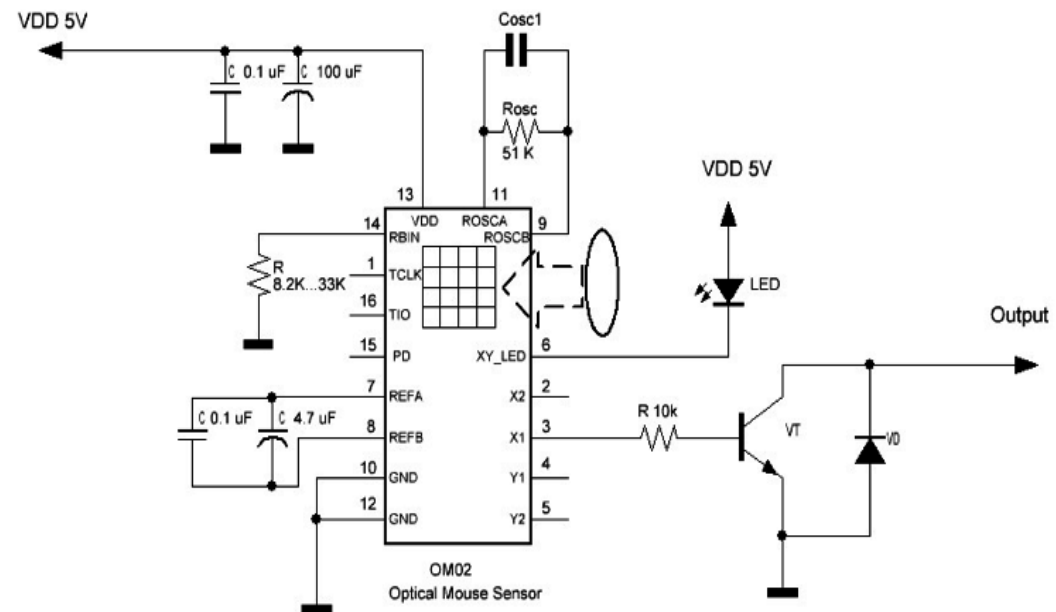
According the IC datasheet, we can use the internal oscillator, in which case Cosc may not be needed. Rosc defines the frame rate: lower values correspond to higher rates.
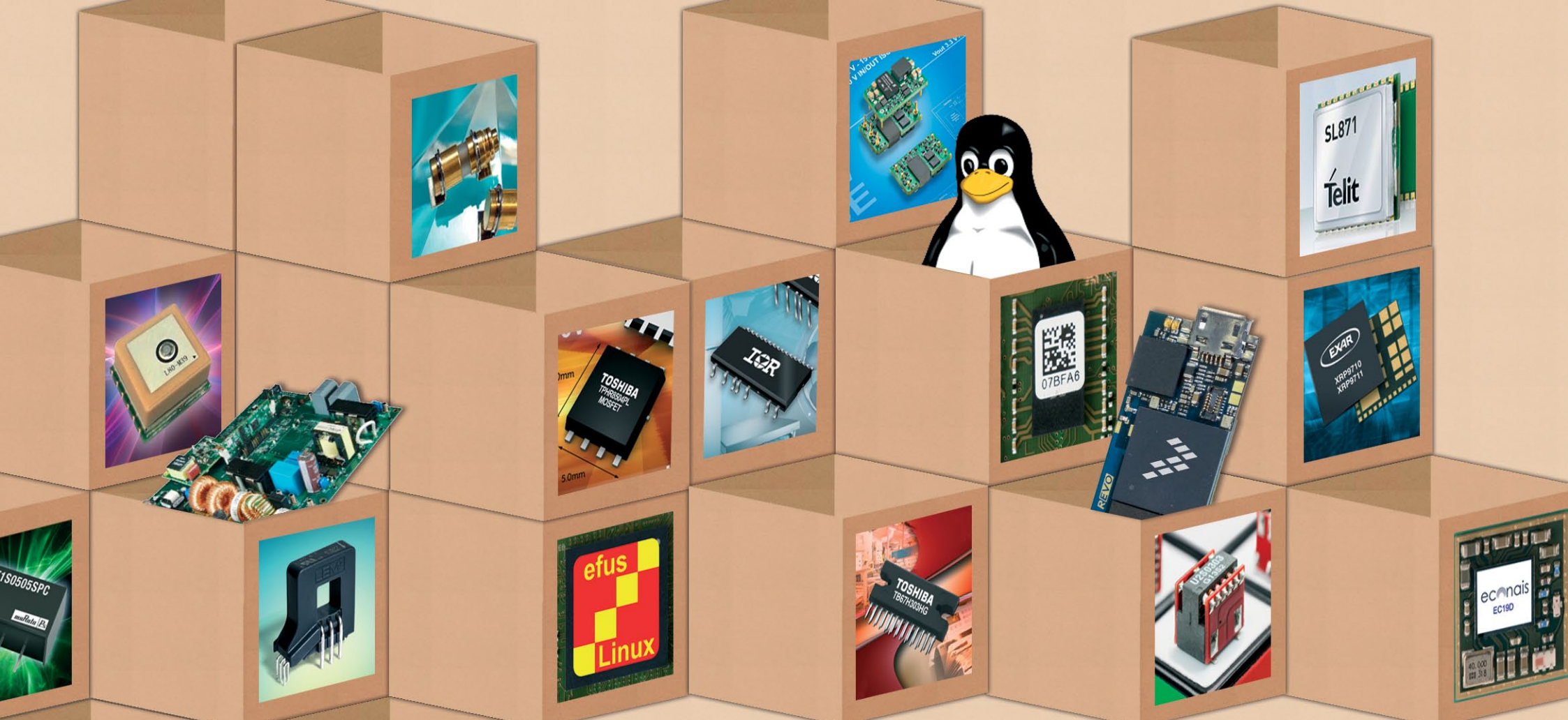
Connecting the X1

where t = 40us

Example: Quadrature Output Waveform (+X motion)

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and X2 outputs to an XOR gate, we can double the data rate, though losing directional information.

Physical realisation

The sensing disk or other surface must have some texture, pattern, scratches, or a brushed finish to get good results for the optical recognition of its surface patterns.

The construction below was successfully applied to provide synchronised movement on assembly lines, and for transporters, labelling equipment, and printing on moving objects. Over 100 units were made, and all continue to work well after several years.

Other sensor ICs are available which will handle different light sources, outputs, speeds, etc. For instance, the PAN3101 CMOS opti-

cal mouse sensor uses SPI, and the PAN101B CMOS optical navigation sensor has both SPI & quadrature outputs.

Example schematics for SPI interface

The sensors with SPI (or USB using one more IC) interfaces don't allow us to track every pulse separately as they send packets of data. For hard real time applications, the sensors with the quadrature output are preferable.

It would be interesting to build an encoder from a wireless computer mouse; and perhaps even more interesting, using the sensor from a digital caliper, as most of them have an I^2C interface. But that's another story.

productroundup

Silicon/software for USB Type-C to DisplayPort cables

Cypress Semiconductor has assembled a complete silicon and software offering for USB Type-C to DisplayPort adapters (dongles). The EZ-PD CCG1-based Type-C to DisplayPort Cable solution enables connectivity between a USB Type-C receptacle and a DisplayPort (DP) or Mini DisplayPort (mDP) receptacle, allowing emerging Type-C notebooks and monitors to be interoperable with older products. Cypress has demonstrated that its Type-C to DP solution is interoperable with the Apple MacBook, the Google Chromebook Pixel, and multiple other systems.

Complete article, here ▶

## Audio DSP chip will produce a better listening experience, says ON

ON Semiconductor and AfterMaster Audio Labs have designed the BelaSigna 300 AM IC that embeds AfterMaster technology, from AfterMaster HD Audio Labs (Hollywood, California) that according to the two companies, will enhance the digital audio listening experience on any consumer device. The chip will operate at 4 mA from a 1.8V source while running AfterMaster HD's algorithms to offer high-fidelity, studio-quality sound to audio-enabled devices and services, using real-time mastering and re-mastering processing technology as well as proprietary Adaptive Intuitive Response mechanisms

Complete article, here ▶

20A hot-swap controller has MOSFET & current sense

LTC4234 is a 20A Hot Swap controller with integrated MOSFET and current sensing, providing a small footprint hot-plug solution for high density circuit boards. The device ensures safe board insertion and removal from live 2.9V to 15V backplanes by controlling an internal N-channel power MOSFET to gently power up bulk capacitors, avoiding sparks, connector damage and system glitches. By integrating the two most critical and largest Hot Swap components – the power MOSFET and sense resistor – the LTC4234 reduces design time and saves board area.
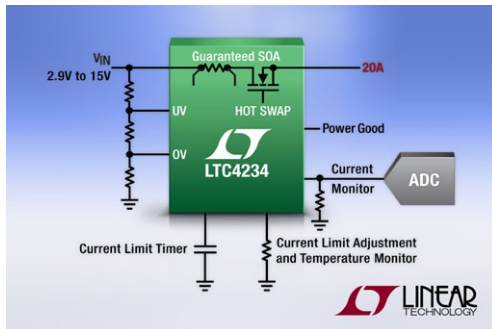
Complete article, here ▶

Power-monitoring IC for single-phase AC

Microchip Technology's MCP39F511 is a highly integrated and accurate single-phase power-monitoring IC, designed for the real-time measurement of AC power, combining the most popular power calculations with advanced features. Allowing for more accurate power measurements, this device is capable of 0.1 % error across a wide 4000:1 dynamic range. Its 512 bytes of EEPROM allow operating-condition storage. The MCP39F511 also includes two 24-bit delta-sigma ADCs with 94.5 dB of SINAD performance, a 16-bit calculation engine, and a flexible two-wire interface.
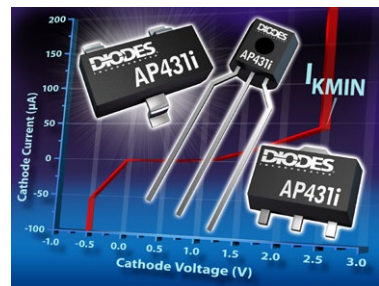
Complete article, here ▶

Shunt regulator betters 431 specs, replaces Zeners

The AP431i adjustable shunt regulator, introduced by Diodes Incorporated, features a 50 µA minimum cathode current that is significantly lower than equivalent industry standard 431 devices. Manufacturers of switch-mode power supplies can target applications that require very low power dissipation, particularly 12V/19V adaptors/chargers. The AP431i three-terminal adjustable shunt regulator features fast turn-on characteristics, a low temperature coefficient and low output impedance. The AP431i has the same electrical specifications as a standard 431, while having an advantage in being able to regulate with a low minimum cathode current.

Complete article, here ▶

SmartMSD simplifies USB file transfer

SEGGER's Smart Mass Storage Device (SmartMSD) uses the proven MSD standard to easily stream files to and from USB devices, by Drag and Drop command. The active file system technology employed in SmartMSD is unique. Once the USB device is connected to the host, files can be read or written to the application without the need for dedicated storage memory. The SmartMSD software analyses what operation is performed by the host and passes this to the application layer of the embedded target, which then performs the appropriate action.
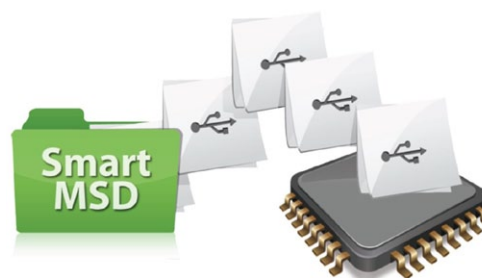
Complete article, here ▶

Debug over USB for system insights in complex SoCs

UltraSoC, provider of advanced debugging and analytic technology for embedded systems, has announced USB-based debugging capabilities within its flagship UltraDebug product. This announcement relates to its technology that allows a single high-speed chip interface – in this case USB 2.0 – to be used simultaneously for both system communication and for analytics applications such as debugging. Future developments will support other standard interfaces, such as Ethernet or PCIe. UltraDebug helps engineers to understand the complex interactions between software and hardware in today's complex chips, which frequently have several billion transistors running tens of thousands of lines of software code. Adding dedicated analytics circuitry to the chip dramatically simplifies the process of debugging – a process which today commonly consumes up to half of the total development time of a large SoC.

Complete article, here ▶

DLP chipset for automotive head-up display

Texas Instruments has introduced a first DLP (Digital Light Processing) chipset for automotive head-up display (HUD) applications. Combining the imaging qualities of DLP technology with automotive reliability, the chipset enables head-up displays with the widest field of view (FOV) available; up to 12 degrees. The chipset gives high brightness, colour and contrast levels and provides manufacturers with a scalable platform. The DLP3000-Q1 chipset consists of a DLP 0.3-inch wide video graphics array (WVGA) digital micromirror device (DMD) and DLPC120 controller.

Complete article, here ▶

productroundup

Signal conditioning for magnetoresistive sensors

ZMDI (Dresden, Germany) has added the ZSSC5101, an automotive-qualified sensor signal conditioning IC for contactless position sensors based on magnetoresistive technology. The ZSSC5101 can directly interface with magnetoresistive sensor bridges such as AMR (anisotropic magnetoresistive), GMR (giant magnetoresistive) and TMR (tunnel magnetoresistive) sensors, enabling up to 360° angle sensors or high-resolution linear motion sensors. The chip automatically compensates for temperature drifts of the sensor, allowing superior accuracy over its full temperature range of -40°C to +150°C.

Complete article, here ▶

10W charger design meets latest specs

Using its InnoSwitch ICs, this reference design from Power Integrations for a 10W CV/CC charger meets DOE-6 and European CoC Version 5, Tier 2 efficiency standards at the end of the cable. RDK-420 is a reference design kit for a 10W CV/CC USB charger based on PI's InnoSwitch-CH family of highly integrated switcher ICs. InnoSwitch ICs combine the primary-side switch together with primary and secondary controllers and feedback circuits into a single, worldwide safety-rated, surface-mount package.

Complete article, here ▶

## Imagination tunes IP for low-power, integrated-wireless IoT connectivity ICs

SoC designers of low-power connected devices can select a modular implementation of wireless LAN (Wi-Fi 802.11n), Bluetooth Smart, or both, on their chip, using Imagination Technology's Ensigma Whisper Cores. The family of cores and peripherals has been shaped for lowest power consumption connectivity IP for wearables and IoT. Imagination designed the Ensigma Whisper flexible connectivity IP family (first release: September 2014) to enable the integration of ultra-low power communications in SoCs that will require extended battery life and low cost points.
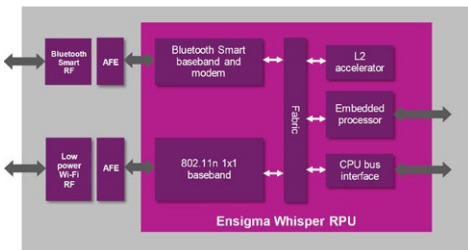
Complete article, here ▶

200W, 98%, 10x14mm buck-boost regulators

Vicor has added to its Picor Cool-Power ZVS Point of Load (PoL) Regulator portfolio with its high efficiency PI3749, PI3751, and PI3755 buck-boost regulators; the DC-DC buck-boost modules provide over 200W and over 98% peak efficiency. By minimising switching losses, Picor's ZVS (zero-voltage switching) topology maintains a high efficiency over the specified Vin range; high frequency operation (up to 2.5 MHz) enables highest power density and fastest transient response. The LGA System in Package (SiP) has integrated controller, power switches and support components.

Complete article, here ▶

productroundup
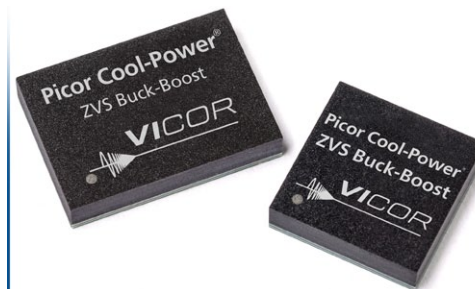
Freescale 9-axis sensor platform shield, with sensor fusion, in distribution

A sensor expansion board for accelerometer, magnetometer and gyroscope, the Freescale 9-axis sensor platform shield is available from distributor element 14; FRDM-STBC-AGM01 features three of the latest sensing technologies incorporated on one board. This 9-axis sensor expansion board for the FXAS21002C gyroscope and the FXOS8700CQ integrated e-compass, is compatible with most Freescale Freedom boards and is supported by the Freescale Sensor Fusion Toolbox. The FRDM-STBC-AGM01 is suitable for a wide range of applications requiring motion, orientation and location.

Complete article, here ▶

Bluetooth Smart sensor beacon integrates accelerometers

I nexpensive Bluetooth beacons with integrated tri-axial accelerometer enable "motion" and "context aware" beacon applications. EM Microelectronic, the semiconductor company of the Swatch Group, has introduced its EMBC02, a combination of sensors with EM's low-cost, low-power and fully certified beacon technology. EMBC02 Series beacons integrate a 3-axis accelerometer enabling a wide range of motion-based beacon applications. By attaching EMBC02 to objects or people, both, proximity and motion, can be monitored by a smartphone or tablet application. EMBC02 can be programmed to transmit proximity and identification data, like standard beacons, but it can also provide motion data.

Complete article, here ▶

Rubidium miniature atomic clock

M icrosemi's enhanced Quantum rubidium miniature atomic clock (MAC) SA.3X family exceeds, the company says, wireless LTE base station and mission-critical defence infrastructure holdover requirements. As one of the smallest, lightest and highest-performing MACs, the enhanced Quantum MAC SA.3X family is based on Microsemi's coherent population trapping (CPT) technology, to meet all traditional, broad market frequency reference application needs. Featuring mechanical robustness and temperature performance, the MAC SA.3X family is only 25% of the volume of the nearest competing clock in the same category.

Complete article, here ▶

EtherCAT slave controller has integrated PHYs for industrial Ethernet

Microchip Technology's LAN9252 is a stand-alone EtherCAT slave controller with two 10/100 PHYs. This highly integrated device's dual 10/100 Ethernet transceivers support both fibre and copper, along with cable diagnostics capabilities. The LAN9252 supports traditional Host Bus and SPI/SQI communication, along with standalone digital I/O interfaces, providing system designers with the flexibility to select from a wide range of microcontrollers when implementing the real-time EtherCAT communications standard in factory-automation, process-control, motor/motion-control and Internet of Things (IoT) industrial-Ethernet.

Complete article, here ▶

EDA INSIGHTS

FINFET IMPACT ON DYNAMIC POWER   ARVIND NARAYANAN

FinFET transistors are now in production at the major foundries, having gone from drawing board to products on the shelf in record time. FinFET adoption has been growing steadily because they deliver better power, performance, and area compared to their planar counterparts. This makes them very compelling for smartphones, tablets, and other products that require long battery life and snappy performance. Figure 1 shows the advantages in speed, power usage, and density of TSMC's 16nm finFET process over two other processes.

When Intel first used finFETs at the 22nm node, they claimed 37% better performance (at the same total power) or 50% power reduction (at the same speed) than bulk, PDSOI, or FDSOI. These numbers are compelling, and continue to improve even down to 14nm, and presumably, beyond.

In terms of power usage, controlling power leakage has been a huge challenge for planar devices, especially at smaller nodes. By raising the channel and wrapping the gate around it, finFETs create a fully depleted channel to overcome the leakage problems of planar transistors. The better channel control of finFETs leads to lower threshold and supply voltages. While leakage is under control in finFETs, dynamic power consumption accounts for a significant chunk of the total power. FinFETs have higher pin capacitances compared to planar transistors, which results in higher dynamic power numbers. According to Cavium networks, "FinFETs bring a 66% increase in gate capacitance per micron compared to 28 nm process, and [are] at the same level [as that] of the 130-nm planar node." Figure 2 charts the gate capacitances of planar and finFET devices.

So what does this mean to the design engineer and how does it change the [IC] design flow from an implementation perspective? Dynamic (aka switching) power needs to become a cost function during optimisation and has to be considered at all the stages of the flow. FinFETs add to the complexity of physical design flow. Tighter design rules and finFET process requirements, such as voltage threshold-aware spacing, implant layer rules, etc., impose restrictions on synthesis, placement, floorplanning, and optimisation engines that directly impact design metrics. And because finFETs are being implemented at 16/14 nm, multi-patterning automatically becomes a part of any design using finFETs, which adds yet another layer of complexity.

Design automation technologies for finFETs need to be finFET-aware to reduce switching power and offer capabilities such as power-aware RTL synthesis, activity-driven placement and optimisation, CTS (clock tree synthesis) power reduction, and concurrent optimisation of both dynamic and leakage. Power optimisation needs to start early in the design flow and the architecture selection needs to be power-friendly to ensure lowest power when the design is realised.

	16FF/28HPM	16FF/20SoC
Speed @ same total power	38 %	20%
Total power savings @ same speed	54%	35%
Gate density	2X	1.1X

Figure 1. *FinFET performance, power, and area advantages (Source: TSMC. Presented at Open Innovation Platform 2014)*

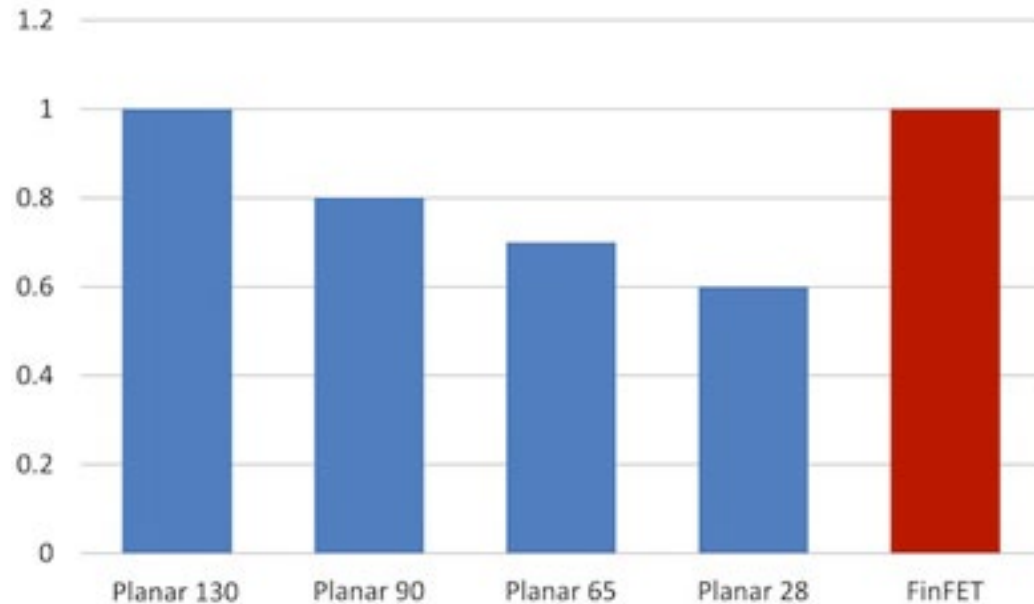## Normalized Gate Capacitance per micron

Figure 2. *FinFET gate capacitance compared to planar processes (Source: Cavium Networks)*

The digital implementation process starts with RTL synthesis. Since finFETs are used in the newest, largest designs, the RTL synthesis engine must have the capacity to handle 100+ million gates with reasonable runtimes. Of course, it must also deliver high-quality results, which can be achieved by running RTL synthesis at the full-chip level when all aspects of the chip can be taken into account. It also helps to be able to run multiple synthesis jobs with different design constraints to explore de-sign alternatives. Having visibility on how the design metrics affect one another lets you make smart trade-offs to meet power, performance, and area metrics.

In order to meet power goals, an implementation flow needs to employ a variety of power-reduction strategies, starting from synthesis and continuing through the physical design flow. The most common strategies include multi-threshold libraries, clock gating, muti-corner/multi-mode (MCMM) power optimisation, pin swapping, register clumping, remapping, and power-density driven placement.

RTL-level power analysis is essential to analyse and fix power problems early in the design flow. Ability to cross probe between RTL, and layout will help identify and debug problems early in the design flow and minimise last-minute surprises. As mentioned earlier, power optimisation needs to be done in all stages of the design flow and should be done concurrently with other design metrics, such as performance and area. The optimisation engine should include dynamic power in its costing and employ transforms such as sizing cells, deleting cells or moving cells to reduce switching wire capacitance.

Design implementation tools for advanced nodes that utilise finFETs must be enhanced and updated with close cooperation from the various foundries. A lot of engineering partnership goes on between the foundries, EDA companies, and mutual customers so that chip designers can take full advantage of each new process node.

FinFETs are already in production and have delivered on the promise of scalability, performance, and leakage power, but have added a lot more complexity to the design implementation flow.

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